High Speed Signal Integrity Capabilities

Read About

High Speed (Gen 3) Fabric Implementation

Next Gen VPX

Introduction

Curtiss-Wright Defense Solutions is a leader in implementation of high speed serial fabric signaling on VPX/OpenVPX™ platforms. We have been there every step of the journey:

- From the introduction of VPX with Gen 1 protocols (e.g. Serial Rapid IO @ 2.5-3.125 Gbaud, PCI Express™ Gen 1 @ 2.5 Gbaud),
- To Gen 2 (e.g. Serial Rapid IO @ 5-6.25 Gbaud, PCI Express Gen 2 @ 5.0 Gbaud),
- Through Gen 3 (40G Ethernet @ 10.3125 Gbaud, Infiniband QDR @ 10.0 Gbaud, PCI Express Gen 3 @ 8 Gbaud),

Developing, introducing and deploying world-leading products at each stage. Work on Gen 4 (PCI Express @ 16 Gbaud) has been ongoing for more than a year, and product timing will be coordinated with silicon availability, among other factors.

Implementation

Implementation of Gen 1 and, to some extent, Gen 2 was relatively straightforward since the VPX connector and infrastructure were designed and rated for these speeds. With Gen 3 came more challenges, in particular the limitations of the VPX connector system such as the relatively high cross-talk at the via footprints of the module and backplane connectors. Curtiss-Wright recognized these limitations very early and worked closely with partners to ensure they could be mitigated when using Gen 3 signaling speeds. We performed extensive signal integrity (SI) simulation and analysis work to understand which mitigations worked, and by what margin. These improvements form the basis of our module and backplane design rules for Gen 3, and substantial testing has shown that they work with enough margin to continue to use the standard VPX connector system (see the following representative data).

Fabric40 Typical SI “Torture Test”

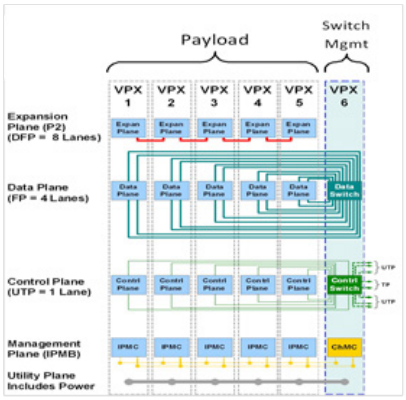

Figure 1: Equipment Tested

Info

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Extra backplane connectors, backplane vias, and 4 ft Meritec™ VPX+ cables for J2 Expansion Plane

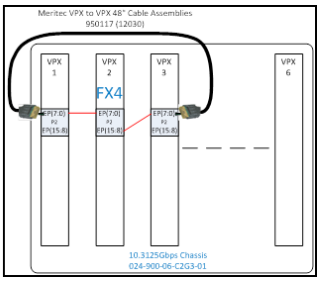

Figure 2: Torture Test Interconnect

CHAMP-FX4 Test Setup
Chassis
Patent-pending Fabric40™ backplane
Fabric40 CHAMP™-FX4 in Slot 3
4 ft Loop-Back Meritec VPX+ Cables in adjacent slots for J2 Expansion Plane
1 ft Loop-Back Meritec VPX+ Cables on RTM for RJ4-6 pass-thru

CHAMP-FX4 Test Conditions
(72) FPGA TX signals are driving simultaneously with PRBS pattern (pseudo-random bit stream)
(72) FPGA RX signals are receiving simultaneously
FPGA TX 10.3 Gbaud at 250mV pk-pk

Fabric40 SI Test Results

Fabric40 Product	Drive Strength	Max Allowed Drive Strength	# of 10.3 Gbaud Lanes	Bit Errors @ 10^{-12} BER	Potential Margin Increase
CHAMP-FX4 (FPGA processor)	250 mV	1200 mV	72	None	~18 dB (7X eye height)
CHAMP-WB DRFM	400 mV	1200 mV	8	None	~17 dB (8X eye height)

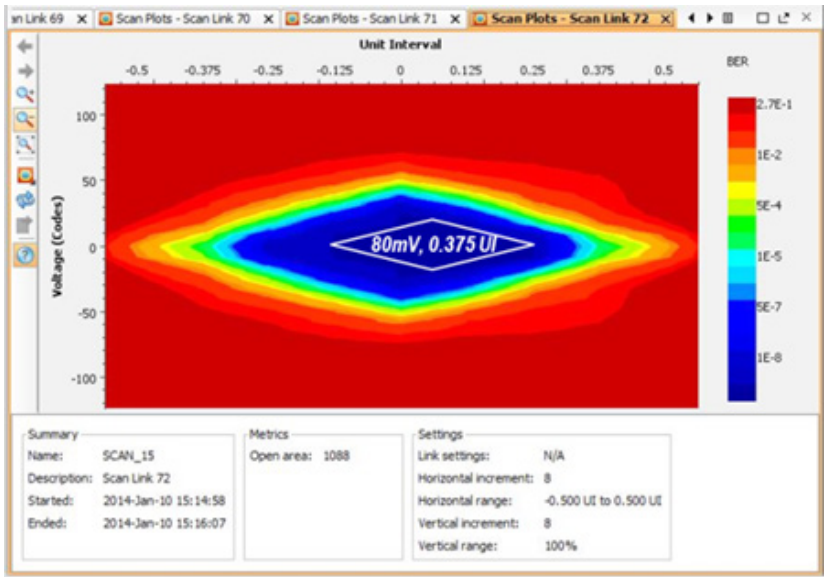

Figure 3: XILINX™ IBERT Eye Diagram for Worst Channel Ultra Low Power TX at Only 250mV pk-pk

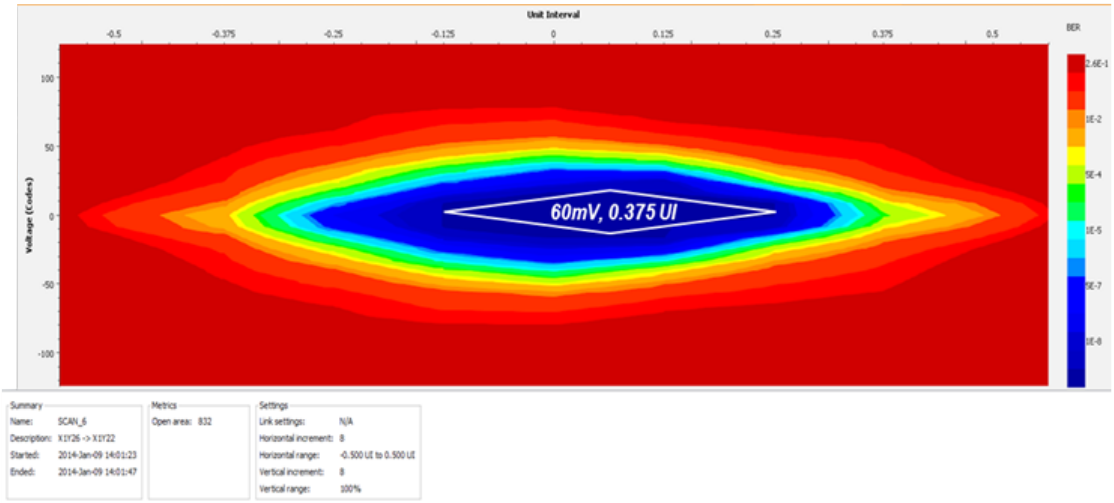

Figure 4: XILINX IBERT Eye Diagram for Worst Channel Ultra Low Power TX at Only 400mV pk-pk

Fabric40 Product	Drive Strength	Max Allowed Drive Strength	# of 10.3 Gbaud Lanes	Bit Errors @ 10^{-12} BER	Potential Margin Increase
CHAMP-AV9 (Intel-based DSP processor)	1000mV	1730mV	16	None	~4.7dB

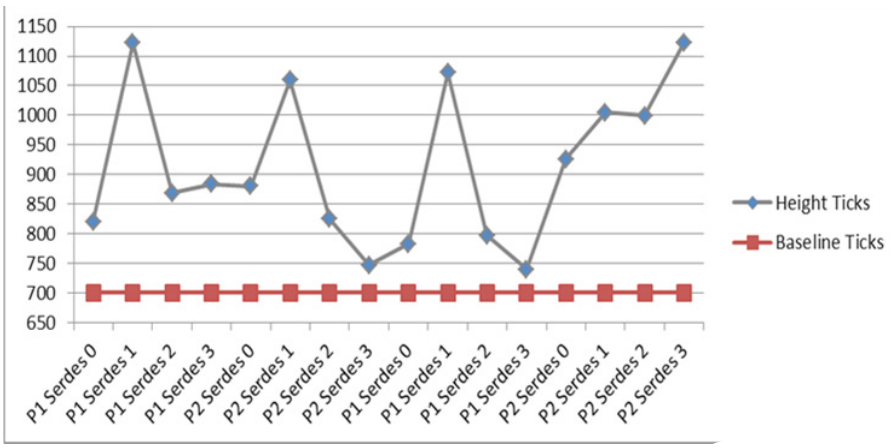

Figure 5: Eye Opening in Height on All Channels

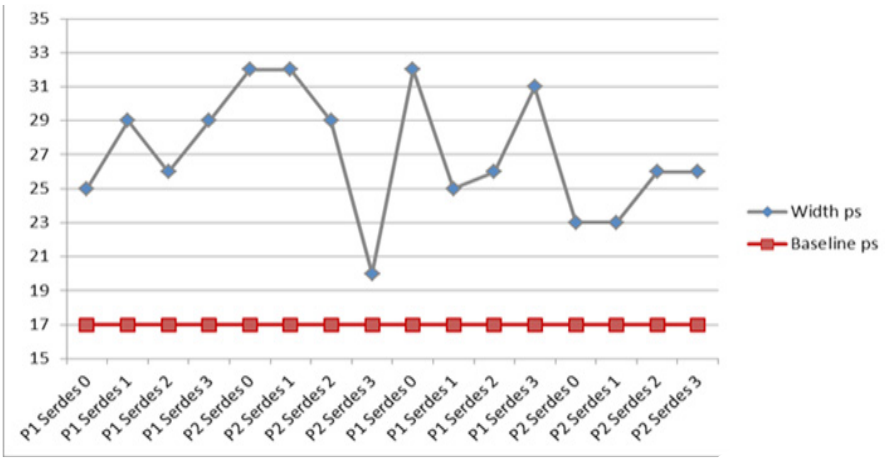

Figure 6: Eye Opening in Width on All Channels

In addition, Curtiss-Wright has been and continues to be a major contributor to the VITA 68 VPX Channel Compliance standard and specifications for Gen 3 (e.g. 40GBASE-KR) signaling implementations. Bob Sullivan (former CTO, Engineered Packaging Products for CWDS) continues to chair this effort, and we continue to have strong ties with Bob.

The Gen 3 successes led us to introduce a portfolio of products under the Fabric40 banner (meaning Gen 3 capable). These products form the hardware basis of our current High Performance Embedded Computing (HPEC) offerings, and are being deployed in other applications as well.

Recently, Curtiss-Wright worked with a defense sector customer on a custom backplane design for 40Gb/10Gb Ethernet. We provided the design guidelines and rules driven from our own module and backplane designs. Initial design guidance was given, and then followed through with full design review and analysis in support of our customer, including on-screen review of the PCB layout and artifacts. Recent test data [that cannot be shared at this time] indicated that 18" of backplane fully supported 40Gb/10Gb signaling, in all slots loaded with modules running 40Gb/10Gb signaling. The eye masks showed significant margin in one to one card tests, as well as fully loaded with crosstalk.

Curtiss-Wright has not limited testing to 10.3125 Gbaud, for example on the CHAMP-FX4 FPGA product, we conducted testing at 11.4 Gbps and 12.5 Gbps, utilizing the Xilinx V7 690T FPGA SerDes [GTH] interfaces. The tests consisted of 72 SerDes running in parallel, through the FX4 PCB transitioning to the backplane via standard VPX connectors, then looping through a 1 foot Meritec Cable. The backplane is from Atrenne Computing Solutions, who purchased the Curtiss-Wright Electronic Packaging Systems group (formerly Hybricon) in 2015. We continue to have strong ties with Atrenne/Hybricon, and share substantial high-speed IP.

Results from the above testing indicate that as the bit rate increases, the margin decreases on the receiver mask area (not surprisingly). The following is an eye mask at 11.4 Gbps, which still indicates an excellent eye diagram.

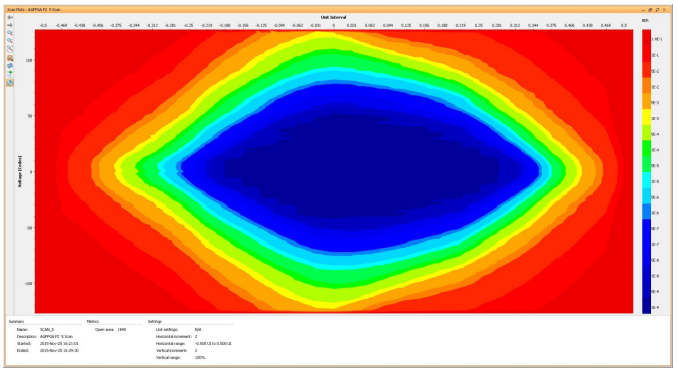

Figure 7: Eye Mask at 11.4 Gbps

For a review of results at 10.3 Gbps and 12.5 Gbps, the data indicates a nominal reduction of eye height. Results were run at 10.3 Gbps, 11.4 Gbps, and 12.5 Gbps. The tests showed that the limitation of the existing VPX connector is around 12.5 Gbps, with some links below eye height requirements (whether this is related to the VPX connector, or the SerDes limitation in the Xilinx FPGA is on ongoing investigation, as part of understanding the next steps in high speed connectivity).

Gen 4

We are not resting on our Gen 3+ laurels. Work on Gen 4 (e.g. PCIe @ 16 Gbaud) and beyond has been ongoing for over a year. We are taking our successful Gen 3 design rules and practices, and adding to them with input from our Signal Integrity (SI) experts, and others such as world-leading SI experts and leading connector manufacturers. The collection of improvements is being analyzed to determine how far the standard VPX connector can be pushed, from a signaling rate perspective.

In parallel, we are investigating modified and new connector systems to determine if and how they could meet the Gen 4 challenge, although we need to be very careful to avoid disruption of the VPX/OpenVPX eco-system that customers have designed in and deployed on numerous programs and platforms. Any connector changes are being carefully scrutinized to avoid impacting the openness of the existing VPX/OpenVPX infrastructure and eco-system.

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Conclusions

It is difficult to forecast what serial fabrics/protocols and interconnects will be used for Gen 5 and beyond, but 100 G Ethernet (25 Gbaud speeds) is very likely to be among the candidates. This may be an inflection point at which optical/fiber signaling may present enough advantages over electronic/copper signaling that it comes into widespread use on VPX/OpenVPX systems. Curtiss-Wright is involved in leading R&D initiatives to ensure that if and when this occurs, the infrastructure will be in place for rugged, reliable, and cost-effective implementations.

In summary, Curtiss-Wright continues to lead the industry in defining, standardizing and implementing high speed signaling interconnects based on open standards. We have also led in providing literature and webinars on the challenges and potential solutions involved with current and future generations of high speed signaling and fabrics.

Learn More

Video: Meeting the Gen3 backplane challenge with OpenVPX and COTS

White Paper: Fabric40 OpenVPX Signal Integrity: Gen3 OpenVPX Backplanes Supporting 10.3 Gbaud Signaling in OpenVPX Systems

Technologies: Signal Integrity Analysis