Radiation Mitigation in Space: A COTS Approach

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Spacecraft Electronics Design

Space COTS

Smart Protection of COTS

Introduction

When it comes to space vehicle design, whether it is a launcher, a re-entry vehicle or a satellite, the tolerance of on-board electronics to radiation effects becomes one of the most challenging aspects of the design. As the risk of equipment failure due to the radiation effects increases with the altitude and flight duration, the tolerance to radiation effects becomes the crucial criteria for selecting the on board equipment and sub-systems.

In recent times, designers of spacecraft systems have been encouraged by funding Agencies to identify ways and means to mitigate against radiation effects within the scope of limited program budgets while not compromising the overall Mission Safety Assurance requirements. This white paper will discuss how a novel approach to radiation mitigation allows the use of commercial off the shelf (COTS) electronics equipment in a radiation environment, thereby lowering the cost involved in the design, certification, manufacture and deployment of such a system.

Radiation – A Major Problem for Space Equipment Designers

Space radiation consists of highly energetic Protons, Electrons and Heavy Ions. Figure 1 shows the two main sources of space radiation – the Sun and galactic cosmic rays.

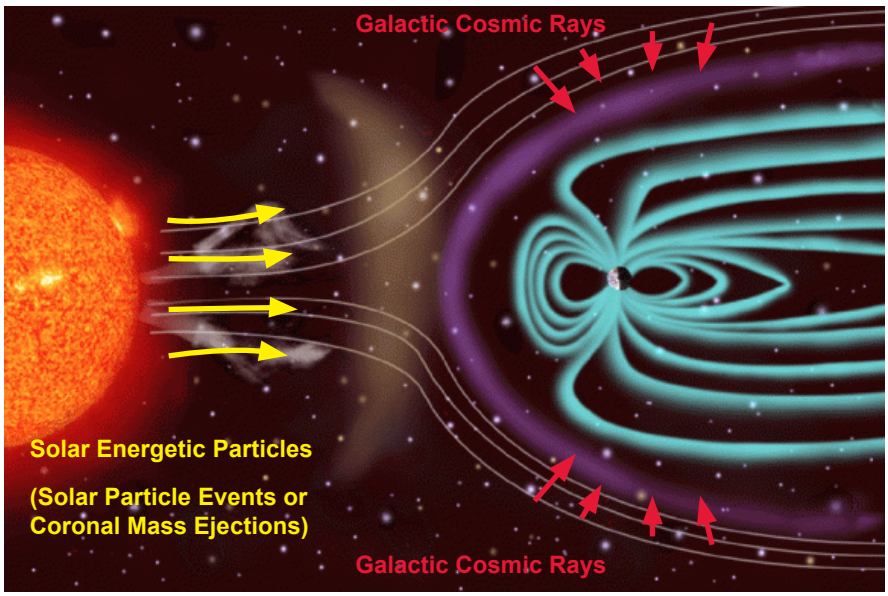

Figure 1: Sources of space radiation

Image Credit: NASA

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Figure 2: Rugged data handling spacecraft electronics

Semiconductor components are essential building blocks of modern spacecraft electronics, including data handling equipment, such as those shown in Figure 2.

As radiation interacts with a semiconductor it produces ionization which effectively increases the conductance of the material. As a result, ionizing radiation creates tiny spikes of electrical current in the material. Cumulatively, these current spikes cause degradation of material characteristics and are known as Total Dose Effects. Individually, they can temporary or permanently disturb the function of a device, a phenomena known as Single Event Effects (SEE).

If you were to think about it in terms of the tire on a car, total dose is the equivalent of general wear-and-tear from road use, whereas SEE is the equivalent of a puncture.

Total dose effects

The amount of radiation dose, i.e. the amount of energy deposited in the material, that results in ionization is called Total Ionizing Dose (TID). The total dose accumulated during a space mission depends on orbit altitude, orientation and duration of the mission.

Ionization of a semiconductor material typically causes very small leakage currents, which can lead to negative long-term consequences. The total dose effects cause a slow degradation of a component's performance, such as threshold voltage shift or decrease in switching speed, and eventually lead to component failure.

Single event effects

The increased density of integrated circuits has resulted in the size of the elementary semiconductor structures shrinking to the level where a spurious current spike produced by a single particle can interfere with the operation of the circuit. These disruptions are commonly known as Single Event Effects (SEE), the three classes of which are:

- **Single Event Upset (SEU)** - occurs when a radiation-induced current causes a memory structure to change its state. This results in a temporary error in device output or its operation and is commonly referred to as "soft error". The device is not damaged and will function properly in the future, but the data processed by the device can be corrupted.
- **Single Event Latchup (SEL)** -occurs when a radiation-induced current activates a parasitic structure (e.g. transistor), which forms an undesired low-impedance path in the semiconductor structure. It disrupts proper functioning of the circuit, and if not corrected, can possibly even lead to its destruction due to overcurrent. The circuit typically remains latched up until it is powered off and afterwards it may continue function properly.
- **Single Event Burnout (SUB)** - occurs in power MOSFETs when the current pulse forward biases the source of the device. If the drain-to-source voltage exceeds the breakdown voltage of semiconductor material, the device can burn out due to the large current that will flow.

When designing electronic equipment for a spacecraft it is essential for the designer to have a good understanding of the environment the spacecraft will operate in as this will influence the scope of their design. This includes an understanding of anticipated total dose as well as the density and energy of particles that may cause SEE during the mission. The equipment is typically tested to one or more resultant effects tests, including TID, proton displacement damage, and single event effects – the test thresholds (Pass / fail criteria) are typically driven by the spacecraft mission requirements.

Radiation Mitigation Techniques

In mitigating radiation effects, the aim is to reduce risk – i.e. an attempt to either eliminate or reduce the probability of a radiation-induced event occurring or to limit the consequences to the system if the event occurs.

There are several common methods employed in electronics design to reduce the effects of radiation on vehicle data handling equipment. Broadly speaking, there are three approaches to address radiation in space electronics design:

1. Improved material hardness
2. Infrastructure design techniques to improve radiation tolerance
3. Software methods to improve radiation tolerance

These include techniques employed at both an electronics level as well as a system-level. The most effective form of mitigation will depend on the scope of the mission under consideration and the expected type and duration of radiation exposure. The different types of mitigation are summarized in Figure 3 and are outlined in the following sections.

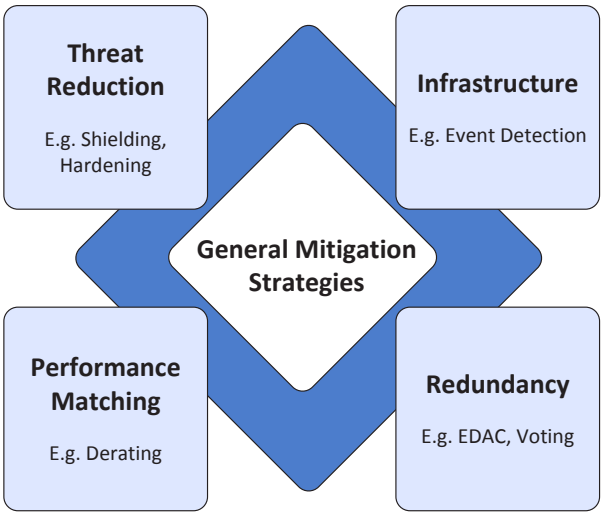

Figure 3: General categorization of system-level radiation mitigation techniques

Cumulative effect mitigation

Total Dose Effects can be minimized with shielding, component de-rating and through conservative circuit design.

Shielding

One option is to introduce a protective 'shield' around an electronic circuit design. Shielding is the practice of reducing the radiation dose experienced by an electronic circuit by blocking the radiation with barriers made of conductive or magnetic materials (e.g. Aluminum or Tungsten).

Shielding is a very effective technique for reducing the impact of electron and low-energy proton dose. However, it generally does not reduce the threat of SEEs caused by high-energy cosmic rays. In fact, thick shielding can have the opposite effect entirely and increase the SEE rate because of the creation of multiple secondary particles due to interactions between the cosmic rays and the shield material.

Shielding also incurs a weight penalty – given the current associated cost of access to space (It cost in the region of $15-20,000 for every kilo of equipment sent to the International Space Station), this may make shielding prohibitive in terms of radiation protection. In addition to this, studies have shown that it is impractical to shield when the cumulative total dose is less than 10,000 Rad.

De-rating & conservative circuit design

Fundamentally, de-rating is the operation of an electronic circuit at less than its rated maximum power in order to prolong its life. In some cases, a device that is functional but has some parameters exceeding specifications after TID testing can be de-rated if the out-of-spec parameters do not affect circuit function and are not radically increasing as the dose is increased.

SEE & SEL mitigation techniques

Event detection and correction

As its name would suggest, latch-up protection is a circuit designed to protect the electronic circuit from a latch-up event. The objective of latch-up mitigation is to allow proper system operation after a latch event. If a latch-up is likely to occur frequently in a mission-critical circuit, then mitigation should include full protection against device damage, automatic recovery from latch-up, and resumption of normal system operation. Depending on the design of the protection circuitry, this may not be sufficient on its own as a mitigation technique.

Redundancy mitigation

Sequential logic such as finite state machines and counters also contain memory elements that may be susceptible to SEUs. These memory elements continuously drive logic, and an upset can easily propagate widely through a circuit. Mitigation through coding is feasible – however, it is rarely used as the encoding and decoding required, as well as the signal routing overhead is considerable.

More commonly, logic memory elements such as flip-flops are triplicated, and a voting circuit is used to continuously detect and correct any SEU. Recent families of radiation-tolerant Microsemi FPGAs, widely used in space electronics, implement this mitigation within the core logic function such that the designer does not need to explicitly include redundant logic.

Redundancy and voting techniques also can be used to mitigate SEUs in microprocessors. For example, multiple microprocessors can be run in lockstep, with all outputs compared and voted to ensure that only proper values are used. However, resynchronization of a processor affected by an SEU is a complex procedure.

An Alternative: Use of Radiation Hardened Components

Previously, we have described several different techniques that individually mitigate against the effects of TID and SEE – there is another option available for electronic system designers. This involves the use of radiation hardened or "space grade" electronic components throughout their designs.

Radiation hardening is the act of making electronic components and systems resistant to damage or malfunctions caused by ionizing radiation in space environments, or even in earth-based applications around nuclear reactors and particle accelerators.

Radiation-hardened components are based on their non-hardened equivalents, with some design and manufacturing variations, normally at the logical function block level, that reduce the susceptibility to radiation damage. For instance, this can be achieved through the use of purpose-developed ASIC cell libraries, (such as the imec DARE180 library) whereby the cells have already been hardened against TID through the use of layout techniques.

Due to the extensive development and testing required to produce a radiation-tolerant design of a microelectronic chip, radiation-hardened chips tend to lag behind their non-hardened counterparts by anything up to 5 years and cost an order of magnitude more. There's also an issue with rad-hard electronics design in that certain components may not be available in rad-hard variants (e.g. high density memories), making it impossible to meet with the functional requirements of the system.

High performance electronics functionality can be very difficult to replicate with rad-hard components – if a non rad-hard component can be used in parallel with an appropriate mitigation technique, this can provide a marked improvement in system performance that may even be mission enabling.

So even though the rad-hard approach to space electronics design will address the functional radiation requirements of a given mission, there is a substantial investment required both in design and manufacture that may not address the budgetary and time constraints of a mission or indeed the functional requirements of the system in question.

A Space COTS Approach

As discussed in the previous section, the lowest-risk method to prevent against radiation is by using hardened components throughout the system design. This will ensure that the system will continue to function as expected with virtual immunity to the nature of the radiation environment. However, it has also been shown that this design technique has several drawbacks, the biggest of which is the cost and time associated with device hardening and with no guarantee that the design will meet with the functional requirements.

At the other extreme, you have the 'buy-and-fly' approach. A designer could build a system from COTS commercial components that meet with the functional requirements and other environmental requirements of the mission (vibration, shock, temperature etc.). The designer knows that there is some radiation tolerance inherent in the design – most commercial components are radiation tolerant to several krad – and hope that the system will continue to function in a radiation environment. The trade-off here is that with this low cost approach, reliability may be compromised. The designer could seek to mitigate the risk associated with their system selection by carrying out a series of ground radiation tests on the equipment to see how it performs

when exposed to the expected mission radiation profile with some design margin. This may be an acceptable approach for low-dose radiation missions where risk of failure is tolerated but in the majority of cases, it isn't a viable option.

However, is there a middle ground between these two extremes where the reliability requirements of a system for a given mission are not compromised while at the same time meeting with the program budget and schedule requirements? This is the Space COTS approach that has been adopted by Curtiss-Wright and which is described in the following section.

The Curtiss-Wright Space COTS System Approach

Flight test heritage

For the last 20 years, Curtiss-Wright has been supplying the Acra KAM-500 – a modular rugged data acquisition and recording system – to the flight test market. The basic building block of these systems is a fixed volume rugged chassis which can accept up to 13 COTS modular data acquisition cards to gather data from a variety of sensor types

Inherent in the design of the KAM-500 are features that actively mitigate against SEU effects. The main feature is what is known as the acquisition cycle. The KAM-500 operates as a collection of synchronized state machines that follow a schedule which occurs once per acquisition cycle. As part of the acquisition cycle, the RAM is refreshed. Therefore any SEUs that occur in RAM are overwritten within one acquisition cycle time. An acquisition cycle time could be anywhere from 100 microseconds up to 2 seconds in length.

Flight test to space electronics – the Smart Backplane

However, standard components are still susceptible to SELs. In order to mitigate against SELs, Curtiss-Wright has designed the 'Smart Backplane' chassis.

The Smart Backplane chassis is a rugged 12-user Slots chassis that has been designed for data acquisition in a radiation-intensive environment. Its design allows the use of COTS interface plug-in modules while at the same time preventing against the harmful effects of ionizing radiation.

Radiation mitigation and the Smart Backplane – a combination of techniques

The chassis backplane is based on a robust design that is not susceptible to SEUs or SELs – this is the only place in the design where "space-qualified" components are used. All plug-in modules are manufactured with commercial components but are protected by the Smart Backplane. It functions in such a way that it can detect an SEL event on a user-module and correct for that event before any damage can be done, thereby ensuring normal data acquisition is resumed without component damage and with minimal data loss. The system recovers from the SEE, and normal operation of the entire data handling sub-system is not compromised, thereby meeting with the mission assurance requirements of a space vehicle.

The system design doesn't seek to prevent radiation events – rather to quickly detect and correct for these events when they happen with no damage to the equipment. And most importantly, the mission safety and reliability requirements are met.

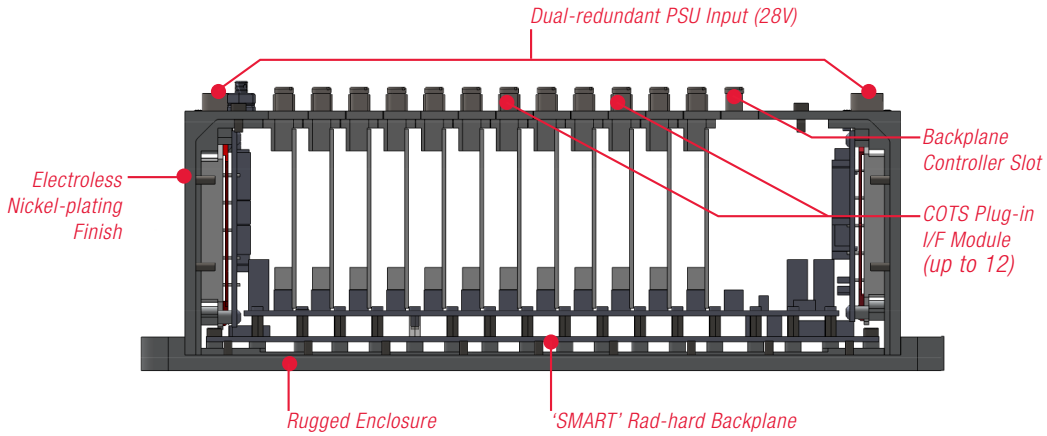

Figure 4: Smart Backplane Design

This design allows the user to have standard plug-in COTS modules in a space environment without the need for those modules to have radiation-hardened components themselves, thereby minimizing the cost of the overall system and leveraging the use of over 100 plug-in modules already designed for data acquisition in aircraft flight testing. The possibilities for radiation-hardened data acquisition are endless. There are a wide range of sensor and actuator interfaces and data buses already available.

Results

In May 2015, radiation testing was carried out on the Smart Backplane design to validate its performance in a radiation environment. The results of this testing can be used to characterize the expected SEE failure mechanisms and SEE rates of the Smart Backplane and the COTS modules it has been set up to protect against radiation.

Proton testing was carried out at Massachusetts General Hospital with a 200 MeV Proton beam up to a fluence of 1E10 protons/cm^2.

Heavy Ion testing was carried out at NASA Space Radiation Lab at Brookhaven National Lab with a 250 MeV Krypton beam generating a Linear Energy Transfer (LET) of 4.2 MeV/mg.cm^2 (Si).

The preliminary results of this testing demonstrated that the Smart Backplane was able to successfully protect itself and user modules from damage during both Proton and Heavy Ion testing. Even though SEL events occurred on the backplane and the modules during the testing (as was to be expected), the Smart Backplane was able to detect and correct for these occurrences, ensuring normal operation resumed with minimal downtime and no component damage. Even with the artificially high exposure levels experienced by the equipment, the data loss rate was <1%.

Summary

Designers of electronics for space applications can take several approaches to designing systems that can survive the effects of radiation. While using fully radiation tolerant designs may yield the most protection, it is also the most expensive option. The Smart Backplane chassis, designed by Curtiss-Wright, allows the use of high-performance COTS data acquisition user-modules in radiation-intensive space applications, lowering the cost of such a system while still meeting with the mission reliability requirements.

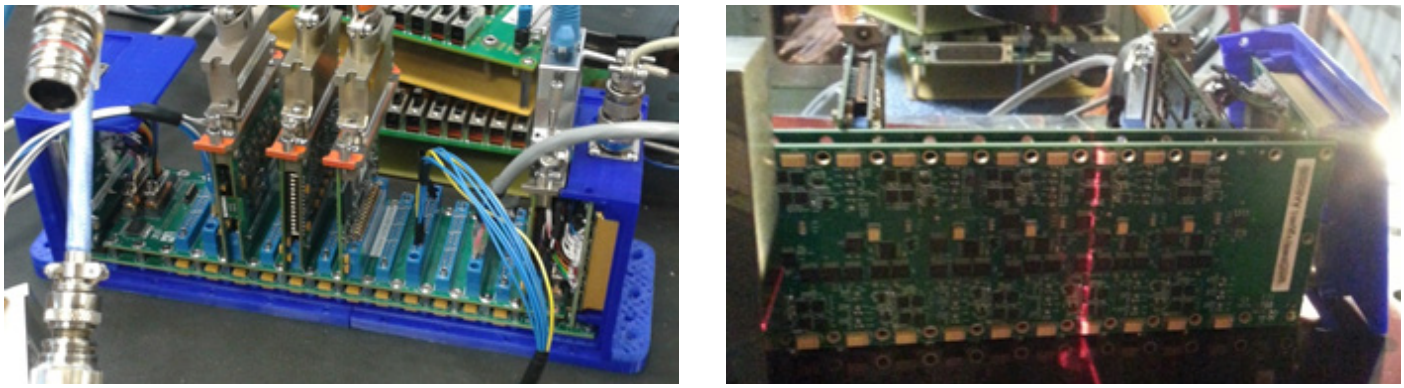

Figure 5: A Smart Backplane DAU being set-up and undergoing proton testing at Massachusetts General Hospital in May 2015

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Learn More

The Smart Backplane Product Sheet

Curtiss Wright Space Brochure

Case Studies:

- The Use of Space COTS for a Re-entry Vehicle
- The Use of Space COTS On-board the ISS

Acknowledgements / Sources

ESA SAVOIR Functional Reference Architecture (TEC-SW/11-477/JLT, dated 31st March 2014)