Understand the FMC Standard and Get the Result You Want

Read About

FPGA Mezzanine Cards (FMCs)

VITA 57

Analog I/O

Mechanical compatibility

Introduction

The FMC standard may seem similar to other mezzanine card formats, like PMC or XMC, but it's not. Put an XMC card on an XMC site and you can generally assume it will work; not so for an FMC card on an FMC site. The FMC standard has huge advantages in terms of I/O throughput and flexibility but matching an FMC card with a carrier has to be done carefully.

It's kind of like building a team for World Cup Football. You want to build the best possible team for international competition and to do that you must be able to choose from a wide pool of players, coming from many different clubs. But highly skilled players are not enough; you need to understand the individual players and all the details; their strengths and weaknesses and when to use them. Get it right and you will achieve great results. Get it wrong and you'll be history.

Figure 1: Successful FMC integration has parallels with building a winning team

Parallels can be drawn with the FMC mix and match format. Get it right and you'll achieve a high performance result. The decisions are more complex than those of the usual mezzanine approach but the rewards are higher.

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I/O Performance and Flexibility

The FMC specification (VITA 57) is powerful: powerful because it provides a platform to couple high performance I/O, usually analog I/O, directly into an FPGA. This performance is built on the direct and intimate coupling of an FPGA and its I/O without standard busses or specific timing constraints getting in the way.

The FMC specification, in the main, doesn't even define the formal connectivity, only how you go about adding connectivity and its limits (maximum number of connections). Some infrastructure is defined, such as where the power supplies are connected (even some of those are optional) and mechanical details such as board outlines, mounting holes and the positioning of the FMC connectors. But defining and formatting the I/O flow is left to the designer.

This freedom is at the heart of the FMC standard's ability to provide high performance, effective solutions – but it needs detailed knowledge and careful design management, which is why there is a strong preference that the FPGA host board and FMC module are coordinated from one source.

The Nuts and Bolts of the FMC Format

The FPGA Mezzanine Card (FMC) specification's foundation is simple. Putting the mechanics to one side, the FMC specification defines:

- **The maximum number of parallel I/O connections.** This is up to 160 signals (or 80 differential pairs) for High Pin Count (HPC) variants and half of that for Low Pin Count (LPC). HPC and LPC use common connectors; the difference is only in the maximum connectivity.
- **The order in which the I/O is allocated if an FMC, or its host, do not have the maximum connectivity.** For example, if the host has 60 connections and the FMC only has 40 connections, the first 40 connections of the host match up rather than using different pins.
- **The maximum number of High Speed Serial (HSS) ports.** Set at up to 10 full duplex.
- **Certain specific core power rails.**
- **A protocol which allows the host card to interrogate the FMC.** Used to determine what the FMC requires for its primary power supply (including range) and then to provide it – if it can.
- **Where clocks are to be provided.**

The FMC specification does not define busses or protocols such as PCIe or Ethernet, for example.

The Challenges

The FMC format challenges are the crux of the necessary integration required between a given FMC and an FPGA host. Below are the areas that should be reviewed by designers in determining FMC-host compatibility.

Electrical compatibility

We won't go into the external performance of any particular FMC here, but let us suppose a candidate FMC has been determined. The next step is to see whether it is compatible with the host. This involves checking the type and amount of I/O. For example, does the host support enough I/O channels, are they fast enough, what I/O voltage is required for the interface and can the host provide a suitable power supply voltage. The first generation of FMCs, and perhaps still the majority, uses 2.5V I/O. However, newer generations of FPGAs are using lower and lower I/O bank voltages, and 1.8V I/O is becoming common.

The next question is, 'Is the FPGA fast enough to support the FMC?' A serially connected FMC might need 10 Gbps serial links, but if the FPGA can only support 3.125 Gbps, that is, of course, a problem.

Mechanical compatibility

Once it has been determined that the FMC and host are electrically compatible, we then move on to the mechanical piece. As we've noted, most FMCs are used for I/O; to be specific, front panel I/O. For air-cooled solutions this isn't a problem, since air-cooled front panels are well-defined through the formal definition of the bezel, which is very similar, though narrower, to PMC and XMC bezels. However, the conduction-cooled specification does not define front panel I/O, as there isn't a standard front panel bezel. Instead, host cards would usually have a stiffening/thermal rib across the front. It is up to the host manufacturer to modify the front rib to include the necessary holes for front panel I/O.

In general, designers of a conduction-cooled FPGA host card do not want I/O to go through the front panel as this will affect the card's rugged characteristics. In addition, conduction-cooled systems usually have very little space to run cables. Conduction-cooled PMC and XMC modules have this same issue, but to a lesser extent as there are more options for non-front panel /IO – at least for digital I/O. Some manufacturers have a removable rib segment but there is no common standard for it and, for hosts that don't need front panel I/O, a removable rib segment is clearly an unnecessary "feature".

Behind the front panel/rib, the FMC specification defines three regions (see figure 2). Region 1 is an optional area and usually used only on FMCs with front panel I/O; this is where the connector would usually be fitted. Region 2 is the primary real-estate and common to all FMCs. Region 3 is optionally used for rugged FMCs; a host for a rugged application provides support that fits to this area and more firmly secures the FMC for enhanced shock and vibration. As most FMCs use all three regions there are not likely to be compatibility issues, but it is worth a check.

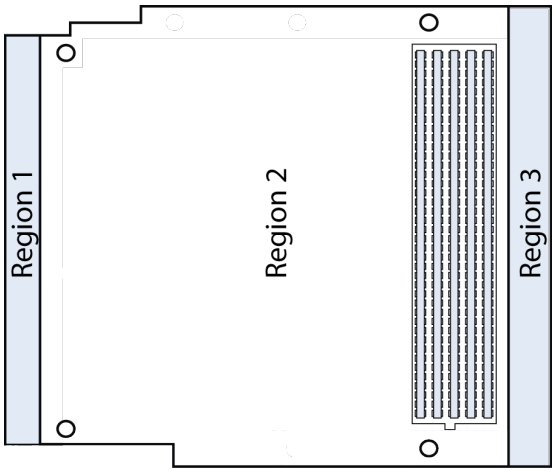

Figure 2: Different regions offered by the FMC specification

There are other mechanical issues to consider such as stacking height and differences in air and conduction-cooled card thermal paths. For stacking height, the FMC specification provides further options, though 10mm in the most common. Conduction-cooled cards can use the edge of the card for cooling to a compliant host. For conduction-cooled cards, this means that no components are fitted in this area. For air-cooled cards, there is the option of having more real-estate for components on the mezzanine, but the risk is that there will be mechanical interference if trying to fit it to a rugged host that supports this thermal path.

Software/HDL compatibility

Given that the FPGA will be directly linked to an I/O device, or whatever function the FMC has, it is clear than the devices are very likely to have very different registers, data interfaces and timing constraints that the HDL and higher level software interfacing to the FPGA will have to deal with. There may even be sophisticated data interface training algorithms to ensure that the interface is robust and isn't affect by timing variations that may be induced by temperature changes or device variations. This is sometimes overlooked for FMCs not specifically designed for rugged applications.

Pre-packaged software and HDL are device and host environment specific. That means quite a bit of code must be developed that is not cross-vendor portable, though some pieces of existing code may be re-used. In addition, the reliability requirements of the defense industry must be met by detailed testing on all specific combinations – especially because of tight timing constraints needed for high-bandwidth I/O and low-latency data processing.

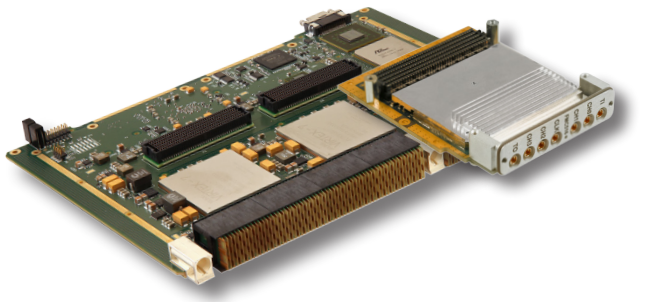

Figure 3: Typical FMC and FMC host; Curtiss-Wright's FMC-516 quad-channel 250 MSPS 16-61t analog input card and CHAMP-FX4 Xilinx Virtex-7 6U OpenVPX module

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Summary

FMCs provides a great deal of freedom for designers to deliver high bandwidth, low latency solutions with minimal hardware, since the standard bus structures are bypassed along with the removal of the interface devices. Typical FMC-based solutions can cope well (on a single FMC) with functionality such as multi-channel/multi-GSPS ADC/DACs or octal 10 Gbps fiber-optics, as well as supporting custom mixed functions. And FMCS provide that flexibility and performance in a relatively small, open-standard form factor.

Given its flexibility, performance and size advantages, it is not surprising that the FMC standard has been widely adopted across the embedded defense industry. There are now a large number of FMC vendors with a wide product portfolio of FMC cards, along with FMC hosts.

While the FMC format works well, there are many things for designers to consider. The primary characteristic to recognize is that FMC isn't really a plug and play format, so board level integration demands careful attention and detailed review.

To help our customers address this issue, Curtiss-Wright has invested significantly in defining and testing a range of FMC -host integrations, insuring that they are suitably robust for the defense market play. As there are a wide variety of FMC vendors, Curtiss-Wright also undertakes integration of third party FMCs onto its FMC hosts, taking into account all of the considerations outlined in this document.

Given Curtiss-Wright's broad experience with FMC integration, why not reduce your design risks by discussing your requirement with us? We are not limited by Curtiss-Wright's portfolio of FMCs but look to engage with the wider market to ensure that the best possible solution can be realized, either through our light integration or complete systems integration capabilities.

Learn More

White Paper: FMC to FMC+: Keeping Up with New FPGAs and Analog I/O

Analog I/O and Digital Receivers

FMC-516: Quad 250 MSPS 16-bit ADC FMC

FMC-518: Quad 500 MSPS 14-bit ADC FMC

FMC-520: Quad 550 MSPS/Dual 1 GSPS 16-bit DAC FMC

FMC-XCLK2: Multi-Channel Clock Generator

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