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Application Note: Incorporating FPGA Processing Directly into Ethernet Networks

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Incorporating FPGA Processing Directly into Ethernet Networks

Introduction

Gigabit Ethernet and other faster Ethernet physical layer interfaces have rapidly become the backbone of many intra-networks in subsystems and entire platforms across the military/aerospace industry. Ethernet is natively included in virtually every general purpose processing architecture and module, and versatile Commercial-Off-The-Shelf (COTS) switching and routing products are now available for this environment. Ethernet is used for command and control, accessing mass storage devices, data recording, sensor data interfaces, audio and video transmission, networking of legacy interfaces, logistics and maintenance support, and more. However, up to this point CPU modules have been the primary directly connected hosts on most military/aerospace Ethernet networks, regardless of the type of data being transmitted. In some cases CPUs are being used as a networking front end for data flows that are ultimately processed using other technologies such as GPUs or Field Programmable Gate Arrays (FPGAs). By directly connecting these non-CPU elements to the network, CPU modules can be relieved of data flow responsibilities and freed to perform other work, while data is funneled directly to the required destination.

Image courtesy of DefenseImagery.mil

Why Connect FPGAs to Ethernet Networks?

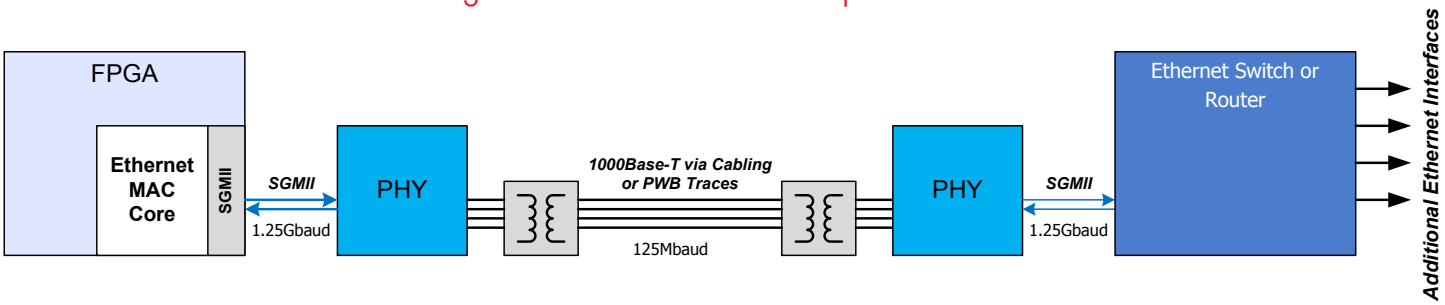
During this same period in the COTS embedded electronics industry, where Ethernet has established a strong foothold as the networking interface of choice, FPGAs have exploded in use as easily customizable circuits for functions ranging from simple glue logic to high performance sensor data processing, and everything in between. We see FPGAs implementing advanced data processing algorithms, performing simple yet highly parallel data transformations, acting as specialty coprocessors to CPU systems, replacing and consolidating legacy interfaces formerly only available with expensive and obsolete ASICs, acting as security engines for data in motion and at rest, along with myriad of other functions as unique as the applications that require them.

One common theme among all of these diverse functions is the requirement for data flows, often of significant bandwidth, to be delivered to and from the FPGA in an efficient and low latency manner. If that data is naturally part of the Ethernet network, requiring a CPU to be a front end for the FPGA introduces unnecessary latency, complexity, and CPU loading that can be eliminated by directly connecting FPGAs to the Ethernet network when appropriate.

1000Base-X: The Natural FPGA Connection

The most common Gigabit Ethernet physical layer standard is 1000Base-T, a four-pair copper cabling standard using Category 5 cables and 5-level pulse amplitude modulation (PAM) signaling techniques to transmit full-duplex gigabit data over a 125 Mbaud channel. This standard is robust, inexpensive to implement, easy to wire, highly immune to external interference, and readily available on most CPU modules in both commercial and military embedded designs. However 1000Base-T also requires special interface chips called phyceivers (PHY) as well as isolation transformers to implement this standard, which means FPGA designs that incorporate Ethernet MAC technology within the FPGA must add these external components somewhere in the design. This requires additional circuit card space, extra power and costs, plus additional FPGA design complexity to manage the out-of-band configuration of the PHY. Figure 1 shows an example of connecting an Ethernet MAC implemented in an FPGA to an external PHY via a multi-gigabit transceiver using the SGMII protocol.

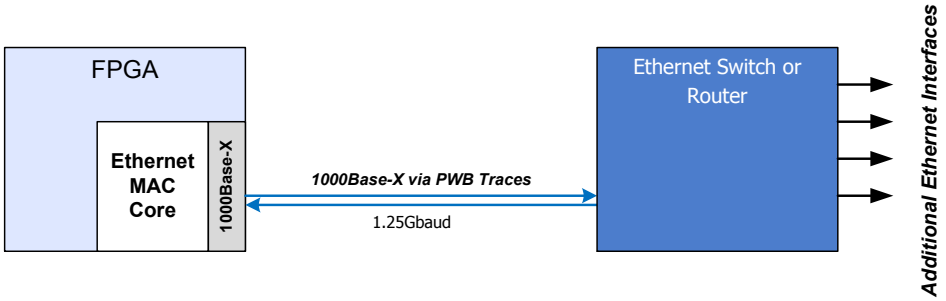
Figure 1: 1000Base-T FPGA Implementation



An alternative to 1000Base-T for FPGA connections would be the 1000Base-X standard. Often referred to as "SerDes" Ethernet (short for Serialization/Deserialization), this standard represents the baseline data layer behind all fiber optic Gigabit Ethernet standards such as 1000Base-SX and 1000Base-LX. 1000Base-X offers the same data speeds and full-duplex connectivity as 1000Base-T, but using half the number of physical signals as 1000Base-T (two pairs LVDS vs. four pairs of 5-level PAM) and not requiring the expensive and space-hogging PHY's and transformers needed for 1000Base-T. The same multi-gigabit transceivers used for the SGMII protocol can be used to directly implement the 1.25 Gbaud 1000Base-X interface straight from the FPGA with no external components except for decoupling capacitors.

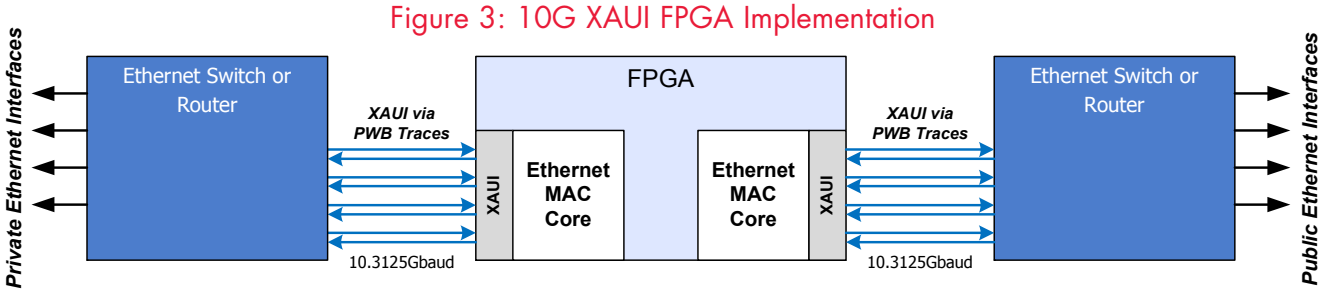
The primary limitation of 1000Base-X vs. 1000Base-T are the signal length and cabling requirements, and increased immunity to external interference which are generally unimportant with intra-system connectivity across differential signaling backplanes such as VPX, where the end-to-end signal path is well defined. Figure 2 shows the simpler design and connectivity of 1000Base-X from an FPGA to a 1000Base-X capable Ethernet switch.

Figure 2: 1000Base-X FPGA Implementation



In addition to Gigabit Ethernet, FPGA intellectual property is available to implement 10 Gigabit Ethernet MACs as well. One of the physical layer standards used to transmit 10G Ethernet is the XAUI standard, which can be implemented directly using four multi-gigabit FPGA transceivers running at 3.125 GBaud. Although a 10 Gigabits/second Base-T standard exists (10GBase-T), the XAUI standard is equivalent to the 1000Base-X standard, with the same circuit size, complexity, power and cost savings whereas 10GBase-T is a much more complex and power hungry interface. For high bandwidth FPGA data flow applications or situations where multiple Gigabit Ethernet interfaces need to be switched into a single FPGA, 10G XAUI Ethernet provides an intra-system interconnect between FPGAs and switches or other network devices to accommodate higher data speeds. Figure 3 provides an example of an FPGA being used to process 10 Gigabits/second of Ethernet traffic between two Ethernet switches.

Figure 3: 10G XAUI FPGA Implementation



Curtiss-Wright 1000Base-X Capable FPGA and Ethernet Products

Curtiss-Wright offers user programmable FPGA modules in a variety of COTS standard form factors including 3U and 6U VPX as well as XMC mezzanine modules. All of these modules provide connectivity off-module with numerous multi-gigabit full-duplex transceivers suitable to implement SGMII, 1000Base-X, or 10G XAUI interfaces. These modules can be connected directly to 1000Base-X or 10G XAUI network connections on various processing modules or Ethernet switch/router modules. Thanks to the proliferation of 1000Base-X and 10G XAUI Ethernet incorporated into the VITA 65 OpenVPX standard, there are many Curtiss-Wright processing and Ethernet switch/router modules with 1000Base-X and 10G XAUI connections, including switch/routers with combinations of 1000Base-X, 10G XAUI, and 10/100/1000Base-T Ethernet all on the same module. While these FPGA products do provide 1000Base-X and 10G XAUI capable connections to the VPX backplane, they often do not map to traditional VITA 65 Control Plane Ethernet port locations, but rear transition modules (RTM) or modifications to standard VPX backplane designs can be used to create the appropriate connections.

CHAMP-FX2 & CHAMP FX3

- 6U VPX FPGA Processors
- Xilinx Virtex-5 or Virtex-6 FPGAs onboard
- 8 to 32 multi-gigabit transceivers routed off card capable of 1000Base-X or 10G XAUI
- Onboard PowerPC CPU with 1000Base-X and/or 1000Base-T Ethernet interfaces off card

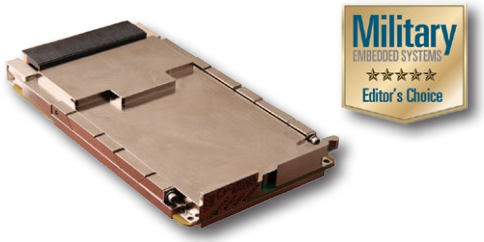
VPX3-683

- 3U VPX Ethernet Switch/Router
- 24 ports 1000Base-X
- 2 ports 10G XAUI
- Full featured managed Layer 2/Layer 3 switch and router

VPX3-450 & VPX3-453

- 3U VPX FPGA Processor
- Xilinx Virtex-5 or Virtex-6 FPGA onboard
- 8 multi-gigabit transceivers routed off card capable of 1000Base-X or 10G XAUI
- Onboard PowerPC CPU with 1000Base-X and/or 1000Base-T Ethernet interfaces off card

VPX3-685



- 3U VPX Ethernet Switch/Router
- 12 ports 10/100/1000Base-T Ethernet
- Options for 8 1000Base-X, 2 10G XAUI, or 4 1000Base-X with 1 10G XAUI
- Full featured managed Layer 2/Layer 3 switch router with Base-X and Base-T combination onboard

XF07 Series XMC Modules

- VITA 42.3 XMC Mezzanine
- Xilinx Kintex 7 FPGA onboard
- 8 multi-gigabit transceivers routed via Pn6 connector capable of 1000Base-X or 10G XAUI
- x4/x8 PCI Express connection to host CPU module

XMC-651

- VITA 42.0 XMC Ethernet Switch
- 8 ports 10/100/1000Base-T Ethernet
- 4 ports 1000Base-X Ethernet
- Lightly managed Layer 2 switch with Base-X and Base-T combination onboard

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In addition to the modules mentioned on the previous page, all current and future generation Curtiss-Wright VPX SBCs and multi-processor VPX modules have options for either 1000Base-X or 1000Base-T Ethernet for 3U VPX and a combination of 1000Base-X and 1000Base-T Ethernet for 6U VPX, in adherence to Ethernet Control Plane requirements for OpenVPX. With this variety of products supporting 1000Base-X and 10G XAUI, often in conjunction with 1000Base-T, direct connectivity of Curtiss-Wright or other FPGA designs to the Ethernet network is easily possible, realizing significant savings in system power, complexity, cost, and increased reliability (MTBF).

Contact Information

To find your appropriate sales representative:

Website: www.cwcdefense.com/sales

Email: defensesales@curtisswright.com

Technical Support

For technical support:

Website: www.cwcdefense.com/support

Email: support@curtisswright.com

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defensesales@curtisswright.com
cwcdefense.com