KAD/CDC/103

Differential ended current-to-digital converter (voltage excitation, 3 kHz b/w) - 24ch at 12 ksps

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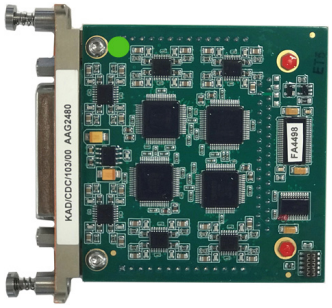

Key Features

- 24 current input channels
- Input range ±22.2 mA
- Accuracy (0.042% FSR typical for input range of ±22.2 mA)
- 16-bit simultaneous sampling on each channel
- Voltage excitation (open-circuit voltage of 12V) for powering the sensor

Applications

- For use with 4 - 20 mA transmitters
- Current measurement

Overview

The KAD/CDC/103 is used to condition and digitize up to 24 differential ended current channels.

At the heart of the KAD/CDC/103 is a hard-wired state-machine that over-samples all channels at a rate between 48 ksps and 96 ksps and digitally filters any noise above the user-programmable cutoff frequency.

This is achieved using cascaded, half-band, finite-impulse-response (FIR) filters followed by an 8th order Butterworth IIR filter with a default cutoff point set at one quarter of the sampling frequency (fc = fs / 4). All signals are sampled simultaneously. Thus, when several channels are sampled at different sampling rates, at the start of an acquisition cycle all channels are aligned.

Voltage excitation is also applied to the sensor.

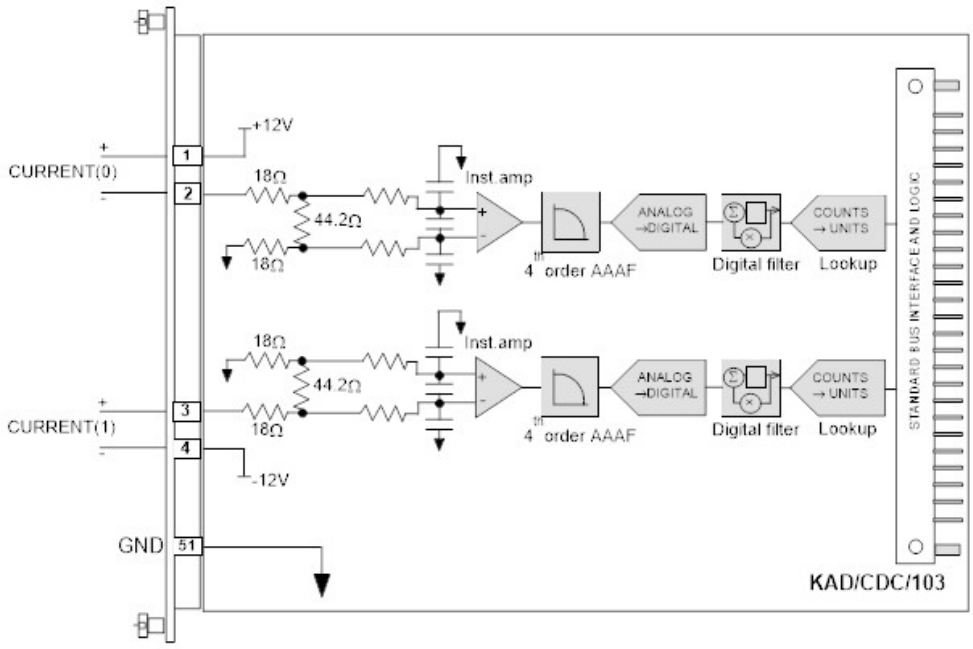

Figure 1: Channels 0 and 1 on the KAD/CDC/103

Specifications

All values provided in the following specification tables are valid within the operating temperature range specified under "Environmental ratings" in the "General specifications" table.

TABLE 1	General specifications				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Slots	–	–	1	–	Can be placed in any user-slot in any combination.
Mass					
	–	90	–	g	
	–	3.17	–	oz	Design metric is grams.
Height above chassis					For recommended clearance requirements see the *CON/KAD/002/CP* data sheet.
bare connector	–	–	11	mm	
bare connector	–	–	0.43	in.	Design metric is millimeters.
Access rate	–	–	2	Msps	Maximum combined access rate for read and write.
Power consumption					
+5V	–	168	180	mA	
±7V	–	0	0	mA	
+12V	–	72	80	mA	Not including excitation, which can be as much as 20 mA × 12.
-12V	–	63	70	mA	Not including excitation, which can be as much as 20 mA × 12.
total power	–	2.46	2.7	W	Particular combinations of chassis and Acra KAM-500 modules may have power or current limitations. For details, see *TEC/NOT/016 - Power dissipation, TEC/NOT/049 - Power estimation*, and the relevant chassis data sheet.
Environmental ratings					See *Environmental Qualification Handbook*.
operating temperature	-40	–	85	°C	Chassis base/side plate temperature.
storage temperature	-55	–	105	°C	

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TABLE 2	Differential ended analog inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	24	–	
Sampling rate					While the sampling rate can be set individually, each must have a power of two times any other (¼, ½ ...2, 4).
CURRENT[23:0]	1	–	12,000	sps	
Input current					
operating range	-22.2	–	22.2	mA	
absolute maximum	-30	–	30	mA	Currents outside of this range can damage input. Note: Do not short Current+ and Current- inputs as the absolute maximum ±30 mA input current limitation is applied. Due to low resistance of the inputs there is no ±40V overvoltage protection implemented.
DC error					
	–	0.042	0.06	%FSR	For input current range of ±22.2 mA.
	–	0.1	0.12	%FSR	For input current range of 4 mA to 20 mA.
Effective number of bits	10.5	11.5	–	bits	
Crosstalk	–	-95	–	dB	
Common mode					
voltage range	-3.5	–	5	V	Operational voltage range. This figure applies to the KAD/CDC/103/NE ordering option only.
rejection ratio	55	65	–	dB	Applies within the above common mode voltage range, $0 \le f \le f_c$. (f_c : filter cutoff frequency)
Analog filter					Analog filter is Butterworth.
poles	–	–	4	–	
filter cutoff -3dB	5.7	6	6.3	kHz	
Digital filter					Digital filter is Butterworth.
poles	–	–	8	–	
filter cutoff -3dB	0.25	–	16	f_s	The maximum value is limited to 3 kHz
0.1dB bandwidth	–	0.8	–	f_c	
aliasing to 0.1dB band	–	–	-72	dB	
aliasing to f_c	–	–	-74	dB	
Filter delay	–	0.66	–	ms	Measured for $f_{in} = f_c = 3$ Hz (f_{in} : input signal frequency). See “Understanding filter delays” on page 5.
Input resistance					KAD/CDC/103
between inputs	260	270	–	kΩ	Module powered off.
Input resistance					KAD/CDC/103/NE
between inputs	-	156.2	–	Ω	Module powered off.
between inputs	-	156.2	–	Ω	Module powered on.
each input to GND	-	13	–	kΩ	Module powered off.
each input to GND	-	12	–	MΩ	Module powered on.

Setting up the KAD/CDC/103

All module setup can be defined in XML using XidML® schemas (see http://www.xidml.org).

Instrument settings

SETUP DATA	CHOICE	DEFAULT	NOTES
Manufacturer	-	-	-
Name	ACRA CONTROL	ACRA CONTROL	Name of manufacturer.
PartReference	KAD/CDC/103	KAD/CDC/103	The instrument part reference.
SerialNumber	AB1234	AB1234	Unique name for each module.
Channels	-	-	-
Current(23:0) Analog Input	-	-	Settings for this channel.
Settings	-	-	-
Filter Cutoff	0.25 0.5 1 2 4 8 16	0.25	Required cutoff point for the filter is the chosen value multiplied by the user sampling frequency. 0.25 is recommended as any higher may lead to aliasing. 1 is the sampling rate.

Parameter definitions

NAME/DESCRIPTION	BASE UNIT	DATA FORMAT	BITS	REGISTER DEFINITION
Current(23:0) Parameters				
Current Current signal data.	Ampere	OffsetBinary	16	R[15:0]

Configurable parameters

Current(23:0)

SETUP DATA	CHOICE	DEFAULT	NOTES
Range Maximum	-0.0222 to 0.0222	0.02	Range maximum for input channel
Range Minimum	-0.0222 to 0.0222	0.004	Range minimum for input channel

NOTE: It is recommended that names are less than 20 characters, have no white space or contain any of the following five characters "/><\.

Getting the most from the KAD/CDC/103

Understanding filter delays

The Acra KAM-500 uniquely samples all signals at the start of an acquisition cycle and at equal intervals of time thereafter. Signals sampled at the same sample rate will always be sampled at the same time independently of how they are stored or transmitted. (This has significant advantages for issues such as time correlation.) However, before signals are sampled they are filtered to remove noise components that might alias. The recommended cutoff point is one quarter the sampling frequency, as this results in the maximum filtering of aliasing frequencies.

The Acra KAM-500 filters signals using over-sampling signal processing techniques. The following figure shows a delay for an 8^{th} order filter where f_c = 1 kHz. All filters cause a delay inversely proportional to the filter cutoff frequency (f_c), so to calculate the delay for other f_c values, multiply the delay by (1 kHz / f_c). The frequency axis then needs to be rescaled to the new f_c by dividing the frequency values by (1 kHz / f_c). For example, an 8^{th} order Butterworth filter with an f_c of 1 kHz delays a 1 kHz signal by 1 ms; a filter with an f_c of 10 Hz delays a 10 Hz signal by 0.1s. The delay for IIR filters (for example Butterworth) varies with the input frequency.

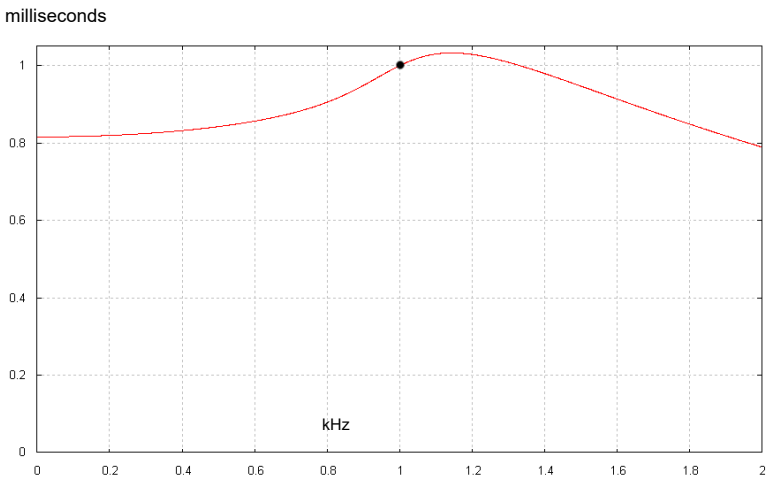

Figure 2: Filter delay for 8^{th} order Butterworth filter where f_c = 1 kHz

The filter delay for the KAD/CDC/103 is:

$$T_D \approx T_A + \frac{1}{f_C} + T_{Butterworth8}(f)$$

T_D is the filter delay

T_A (analog filter delay) ≈ 0

Transducer excitation

The standard version of the module, KAD/CDC/103, provides 12V transducer excitation. The transducer must be connected to the module as shown in the following figure.

NOTE: All even channels of the card are powered from a +12V rail (as per the channel 0 depiction) and all odd channels are powered from a -12V rail (as per channel 1). This is done to maximize the number of cards that can be placed into one chassis and also to ensure even loading and stability of the chassis power supply.

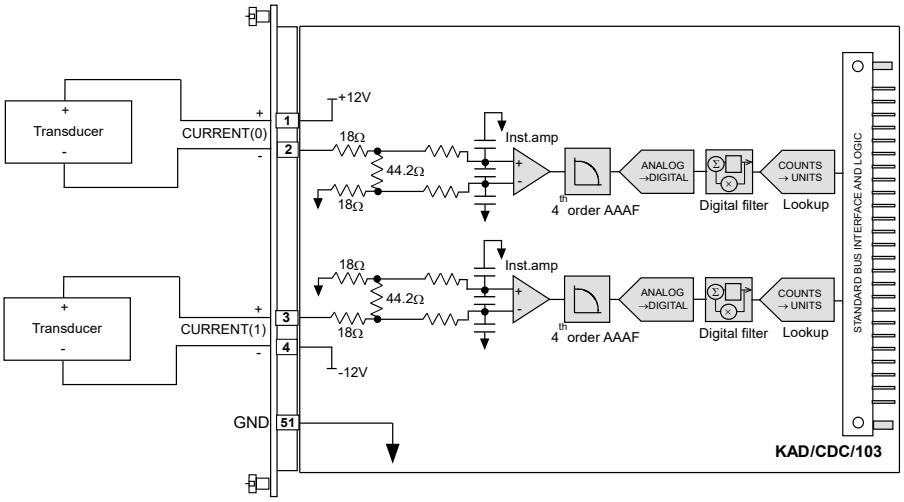

Figure 3: KAD/CDC/103 with transducers connected to channels 0 and 1

The KAD/CDC/103/NE variant does not provide excitation. Transducers must be connected to the module as shown in the following figure.

NOTE: All channels are of the same topology, so only channel 0 is shown.

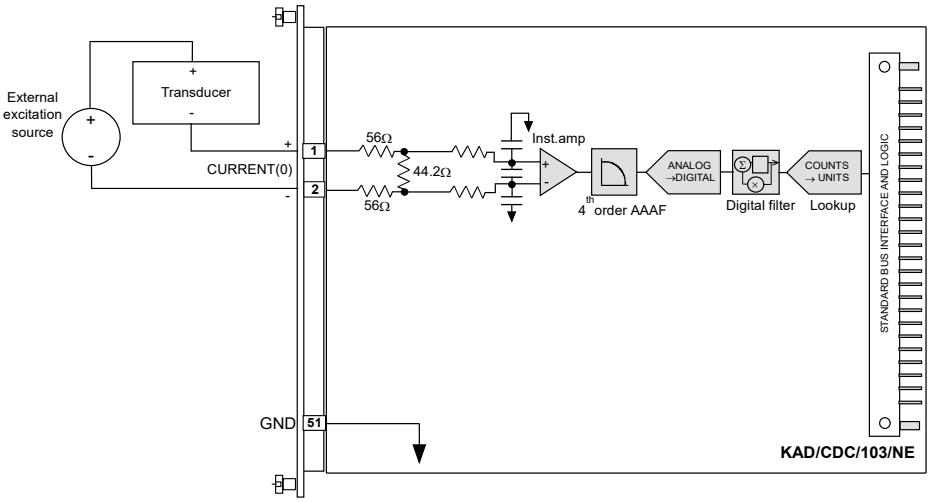

Figure 4: KAD/CDC/103/NE with a transducer powered by an external excitation source connected to channel 0

Connector pinout of the KAD/CDC/103

PIN	NAME	DESCRIPTION	COMMENT
1	CURRENT(0)+	Differential ended analog inputs	Analog input
2	CURRENT(0)-	Differential ended analog inputs	Analog input
3	CURRENT(1)+	Differential ended analog inputs	Analog input
4	CURRENT(1)-	Differential ended analog inputs	Analog input
5	CURRENT(2)+	Differential ended analog inputs	Analog input
6	CURRENT(2)-	Differential ended analog inputs	Analog input
7	CURRENT(3)+	Differential ended analog inputs	Analog input
8	CURRENT(3)-	Differential ended analog inputs	Analog input
9	CURRENT(4)+	Differential ended analog inputs	Analog input
10	CURRENT(4)-	Differential ended analog inputs	Analog input
11	CURRENT(5)+	Differential ended analog inputs	Analog input
12	CURRENT(5)-	Differential ended analog inputs	Analog input
13	CURRENT(6)+	Differential ended analog inputs	Analog input
14	CURRENT(6)-	Differential ended analog inputs	Analog input
15	CURRENT(7)+	Differential ended analog inputs	Analog input
16	CURRENT(7)-	Differential ended analog inputs	Analog input
17	CURRENT(8)+	Differential ended analog inputs	Analog input
18	CURRENT(8)-	Differential ended analog inputs	Analog input
19	CURRENT(9)+	Differential ended analog inputs	Analog input
20	CURRENT(9)-	Differential ended analog inputs	Analog input
21	CURRENT(10)+	Differential ended analog inputs	Analog input
22	CURRENT(10)-	Differential ended analog inputs	Analog input
23	CURRENT(11)+	Differential ended analog inputs	Analog input
24	CURRENT(11)-	Differential ended analog inputs	Analog input
25	CURRENT(12)+	Differential ended analog inputs	Analog input
26	CURRENT(12)-	Differential ended analog inputs	Analog input
27	CURRENT(13)+	Differential ended analog inputs	Analog input
28	CURRENT(13)-	Differential ended analog inputs	Analog input
29	CURRENT(14)+	Differential ended analog inputs	Analog input
30	CURRENT(14)-	Differential ended analog inputs	Analog input
31	CURRENT(15)+	Differential ended analog inputs	Analog input
32	CURRENT(15)-	Differential ended analog inputs	Analog input
33	CURRENT(16)+	Differential ended analog inputs	Analog input
34	CURRENT(16)-	Differential ended analog inputs	Analog input
35	CURRENT(17)+	Differential ended analog inputs	Analog input
36	CURRENT(17)-	Differential ended analog inputs	Analog input
37	CURRENT(18)+	Differential ended analog inputs	Analog input
38	CURRENT(18)-	Differential ended analog inputs	Analog input
39	CURRENT(19)+	Differential ended analog inputs	Analog input
40	CURRENT(19)-	Differential ended analog inputs	Analog input
41	CURRENT(20)+	Differential ended analog inputs	Analog input
42	CURRENT(20)-	Differential ended analog inputs	Analog input
43	CURRENT(21)+	Differential ended analog inputs	Analog input
44	CURRENT(21)-	Differential ended analog inputs	Analog input
45	CURRENT(22)+	Differential ended analog inputs	Analog input
46	CURRENT(22)-	Differential ended analog inputs	Analog input
47	CURRENT(23)+	Differential ended analog inputs	Analog input
48	CURRENT(23)-	Differential ended analog inputs	Analog input
49	DNC		Do not connect
50	GND	Internal ground	
51	GND	Internal ground	
52	CHASSIS	Chassis	Double-density connector only

Ordering information

PART NUMBER	DESCRIPTION
KAD/CDC/103	Differential ended current-to-digital converter (voltage excitation, 3 kHz b/w) - 24ch at 12 ksps
KAD/CDC/103/NE	Differential ended current-to-digital converter (3 kHz b/w) - 24ch at 12 ksps (without excitation)

By default, the standard mating connector (CON/KAD/002/CP), is included with each module in the shipment. Its part number will be added to the Confirmation of Order unless an alternative option is specified (see the *Cables* data sheet).

Revision history

REVISION	DIFFERENCES	STATUS
KAD/CDC/103	First release	Recommended for new programs

Supporting software

SOFTWARE	DETAILS
DAS Studio 3	User interface for setup and management of data acquisition, network switches, recorders and ground stations in an integrated environment

Related documentation

DOCUMENT	DETAILS
DOC/DBK/001	Acra KAM-500 Databook
DOC/HBK/002	Environmental Qualification Handbook
DOC/MAN/030	DAS Studio 3 User Manual
TEC/NOT/016	Power dissipation
TEC/NOT/049	Power estimation

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This document was reviewed on 4/12/2020 and does not contain technical data.