CHAMP-WB

Xilinx Virtex-7 6U OpenVPX Module

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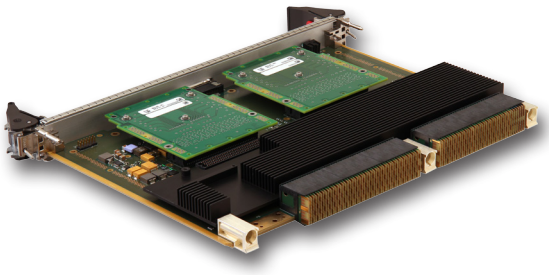

Key Features

- OpenVPX™ (VITA 65) MOD6-PER-4F-12.3.1-8; MOD6-PER-1Q-12.3.5-2, VPX REDI (VITA 48 option)
- Single user-programmable Xilinx Virtex-7 FPGAs (X690T or X980T), with DDR3L SDRAM
- Two Mezzanine sites with support for enhanced FMC (VITA 57)
- 20 x backplane SerDes capable of 10.3 Gbps each
- Onboard PCIe Gen3 switch

Applications

- DRFM
- Electronic warfare
- Radar processing
- Signal Intelligence (SIGINT)
- Wideband Communications
- Image processing
- Sensor processing

Overview

The CHAMP-WB (wide-band) is one of Curtiss-Wright Controls Defense Solutions' family of user-programmable Virtex®-7 FPGA-based computing products, designed to meet the needs of challenging embedded high-performance digital signal and image processing applications. The CHAMP-WB is targeted specifically at wide-band, low latency applications that require large FPGA processing, wide input/ output requirements, with minimal latency. When combined with the TADF-4300 module, featuring 12 GS/s 8-bit ADC technology and 12 GS/s 10-bit DAC technology from Tektronix, an extremely high performance wide-band DRFM system can be created. Alternatively, the CHAMP-WB can be populated with standard ADC, DAC or mixed ADC/DAC FMCs on to support various applications. The CHAMP-WB couples the dense processing resources of a single large Xilinx Virtex-7 FPGA with two high-bandwidth mezzanine sites on a rugged 6U OpenVPX™ (VITA 65) form factor module. The CHAMP-WB complements this processing capability with a data plane directly connected to the FPGA with support for Gen2 Serial RapidIO® (SRIO). 10.3 Gbps Aurora links can also be supported between FPGA cards. Alternate fabrics can also be supported with different FPGA cores. A Gen3 PCI Express® (PCIe) switch connected to the Expansion Plane provides a way for a single host card, such as the VPX6-1957 or CHAMP-AV8, to control multiple CHAMP-WB cards without utilizing data-plane bandwidth. Two 64-bit 4 GB DDR3L memory banks provide 8 GB of on-card data capture or pattern generation capability. An auxiliary x4 SerDes link and 16 LVDS pairs provide additional I/O capability. The two mezzanine sites support standard FMCs and have an additional connector to provide enhanced bandwidth and capability. The extra connector provides at least another 48 differential pairs each as well as extra clocking, power and control signals. Running up to 600 MHz DDR, there is support for over 19 GB/s of data I/O on each mezzanine site. Additional clocking and synchronization signals have been routed to the backplane to provide additional flexibility. Furthermore, one of the FMC sites has an option to take up to eight of the backplane SerDes and rout them to the mezzanine site to support new JESD204B serial I/O or fiber-optic FMCs. This site can also support QSFP or SFP based FMCs.

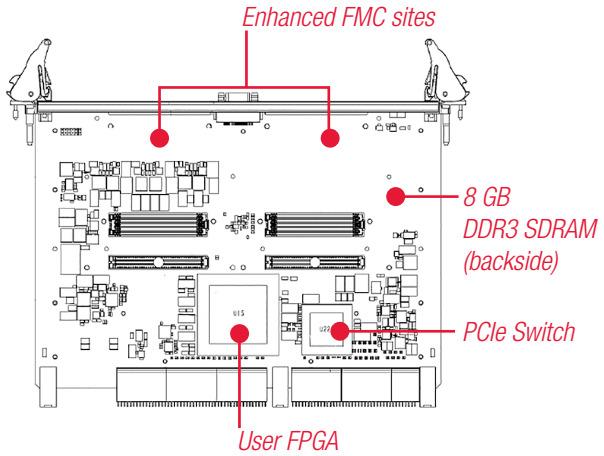

Figure 1: CHAMP-WB key features

Specifications

FPGA

- Device: Xilinx Virtex-7, X690T, X980T
- Number of FPGAs: 1
- Memory (per FPGA): 2 x 4 GB DDR3 SDRAM (64-bit data paths)
- Connectivity
  - 16 x GTH RocketIO to data plane (P1) (max 10.3 GHz)
  - 4 x GTH RocketIO to user plane (P4) (max 10.3 GHz)
  - 4 x Gen3 PCIe from FPGA to Gen3 PCIe switch with two 8 x Gen3 PCIe connections to expansion plane (P2)
  - 16 x LVDS differential pairs to backplane (P3)
- Configuration: JTAG, using onboard QSPI flash, tandem configuration via PCIe, SW update of QSPI flash

Mezzanine sites

- FMC/VITA 57
  - 80 differential pairs
  - 8 bidirectional SerDes pairs as build option for site 2 (replaces x8 backplane connections)
  - I2C
  - 4 x clock pairs

  Note: Site 1 uses serial signals as 20 optional additional LVDS signals
- Auxiliary
  - Connector Site 1
    - 60 differential pairs (X690T) (32 diff prs X980T)
    - SPI
    - Backplane clock
    - Backplane sync
  - Connector Site 2
    - 48 differential pairs
    - SPI
    - Backplane clock
    - Backplane sync

PCI Express

- Connectivity: backplane (two x8 Gen3 on P2), all at 8.0 Gb/s
  - Connection to FPGA is x4 Gen3 PCIe
  - Permits multiple cards to be controlled by single host

Backplane

- Compliance
  - VPX (VITA 46) and VPX REDI (VITA 48)
  - OpenVPX MOD6-PER-4F-12.3.1-8
  - OpenVPX MOD6-PER-1Q-12.3.5-2

  Compatible with the following profiles:
  - OpenVPX SLT6-PAY-4F1Q2U2T-10.2.1
  - OpenVPX MOD6-PAY-4F1Q2U2T-12.2.1-11

  Note: Ethernet pins are reserved for possible future processor option and are not used on this variant
- Connectivity
  - P0: Power and CFPGA utility signals (I2C)
  - P1: 4 x data plane x4 to FPGA (SRIO/Aurora/others)
  - P2: 2 x8 Gen3 PCIe to PCIe switch
  - P3: 16 LVDS pairs to FPGA 1, clock, sync
  - P4: x4 RocketIO to FPGA
  - P5: JTAG
  - P6: Unused (VITA 67.2 option)

FPGA host interface

- Connectivity: PCIe host interface from expansion plane

System control node

- Device: Altera Max V CPLD (5M2210ZF256I5N)
- Connectivity
  - I2C interface to FPGA
  - I2C interface from backplane (P0)

Software/HDL code

- Operating system
  - VxWorks 6.9 with FPGA toolkit: DSW-474-FPGA-VxW
  - Fedora Linux with FPGA toolkit: DSW-474-FPGA-LNX

Standards

- Compliance: VITA 46.0, 46.3, 48, 57.1, 65

Miscellaneous

- Power (estimated)
  - 5V (0W)
  - +12V (typical 60W, max 80W at 71°C, full load, mezzanines not included
  - Max expected power permitted per FPGA at max temp is 45W (estimated)
- Cabling
  - CBL-474-FPL-000: front panel cable, also can be used on RTM
  - CBL-474-iPASSHD: x4 bidirectional SerDes cable for use with RTM SerDes connections
- Weight
  - Air-cooled: 1.75 lb (794 g)
  - Conduction-cooled: 2.4 lb (1090 g)
- RTM: RTM6-474-000

Environmental

TABLE 1 Environmental specifications

QUALIFICATION		COMMERCIAL	RUGGED	
			AIR-COOLED	CONDUCTION-COOLED
		L0	L100	L100
Temperature	Operational (at sea level)	0 to +50°C (15 CFM air flow)[2]	-40 to +71°C (20 CFM air flow)[2]	-40 to +71°C (card edge temp)[3]
	Non-operational	-40 to +85°C	-50 to +100°C	-55 to +100°C
Vibration	Operational (Random)	-	0.04 g^2/Hz	0.1 g^2/Hz
Shock (operational)		-	20 g peak, 11 ms half sine	40 g peak, 11 ms half sine
Humidity (operational)		5-95% non-condensing	Up to 95%	Up to 95%
Altitude[4] (operational)		-	-15,000 to 60,000 ft	-15,000 to 60,000 ft
Conformal coating[5]		No	Yes	Yes

Notes:

1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate shall be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)

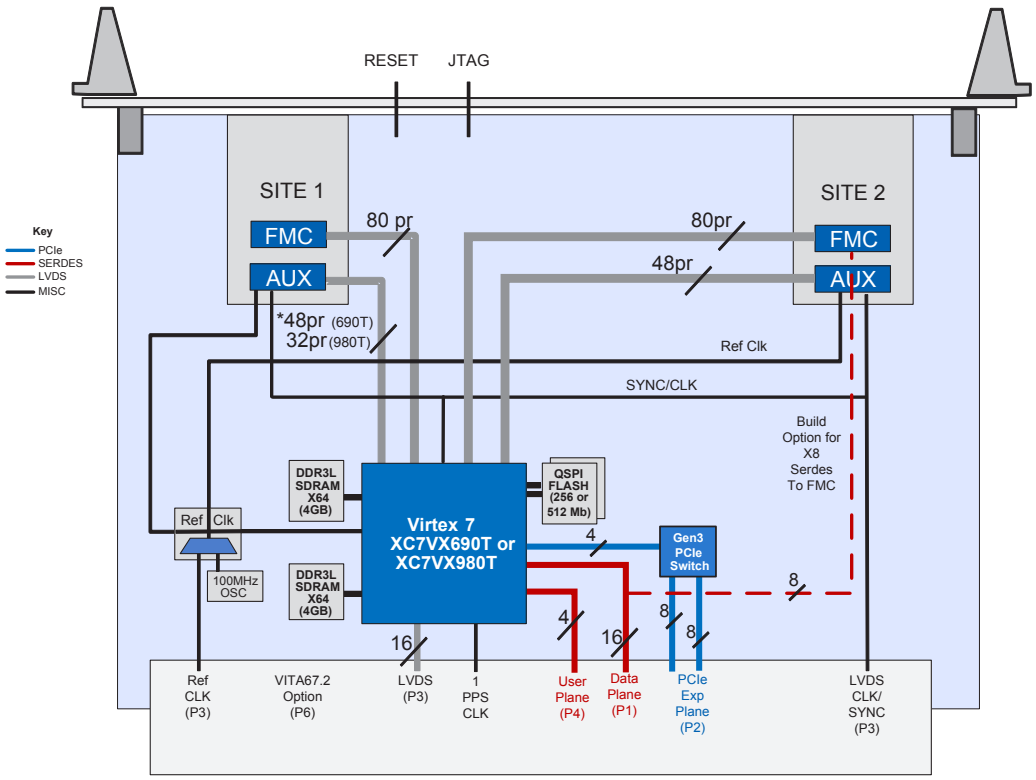

Figure 2: CHAMP-WB block diagram

Xilinx Virtex-7 FPGAs

FPGAs provide parallel processing capabilities, reducing processor count and system size. Operations such as FFTs, FIR filters and other fixed-point and/or repetitive processing tasks are highly suited for placement inside FPGAs.

At the heart of the CHAMP-WB is a single Xilinx Virtex-7 FFG1930 package FPGA, one of the largest FPGAs in the Virtex-7 family. This package is 45 mm x 45 mm and supports 1000 SelectIO pin and 24 high speed SerDes pairs. The -2 speed grade is used by default to provide the maximum performance over the full industrial temperature range. However other options are available. The two FPGA die supported are the X690T and the X980T. Because the X980T -2 speed grade device is only offered for commercial temperature ranges, this variant of the card is only offered as a commercial grade (L0) card. The 'E' version of this FPGA is used to minimize leakage current.

The X690T and X980T devices offer over 690K and 979K logic cells respectively, providing an option for over 2X the capacity of the largest DSP Virtex-6 device. The Virtex-7 slice is the same 4-LUT, 8-FF architecture as was used on the Virtex-6. One change is that the POR (Power-on-Reset) and PROG (Program) signal now clears both LUT RAMs and SRLs. Optimizations have been made to the routing interconnect logic and with the routing tools. This results in a more compacted design within an area of the FPGA allowing much better utilization of the FPGA logic resources.

DSP slices have been increased to 3600, almost double the number of DSP slices available in the largest DSP Virtex-6 device. The DSP slice is the exact same architecture as on the Virtex-6, so any Virtex-6 designs utilizing the DSP blocks can be ported directly.

BlockRam has been increased to approximately 53 Mb in both of these devices which is about 40% more than what was available in the SX475T Virtex-6 device. The BlockRam architecture maintains the same dual 18Kb or single 36Kb block structure. They can be configured as single or dual port memories and contain built-in FIFO logic and 64-bit ECC. One new feature is the ability to disable power to unused memories.

FPGA resource summary

The following table summarizes the amount of different FPGA resources with the different FPGA options available for the CHAMP-WB. This information is directly from Xilinx datasheets.

TABLE 2 CHAMP-WB FPGA resource

RESOURCE		X690T	X980T
Logic resources	Slices	108,300	153,000
	Logic cells	693,120	979,200
	CLB flip-flops	866,400	1,224,000
Memory resources	Max. dist. RAM (kbits)	10,888	13,838
	Block RAM/FIFO w/ ECC (36 kbits each)	1,470	1,500
	Total block RAM (kbits)	52,920	54,000
Clock resources	Clock Management Tiles (CMT) (1MMCM+1PLL)	20	18
Embedded hard IP resources and speed grades	DSP48E slices	3,600	3,600
	PCIe endpoint blocks	2	2
	Speed grade	-2C, -3E	-2E*
	RocketIO GTH (run at 10.3 Gbps or lower)	24	24

Note: Offered as commercial grade only.

FPGA architecture

The FPGA node on the CHAMP-WB has been architected to maximize I/O bandwidth and minimize latency for sense-and-response applications as well as providing large DDR3L memory banks. Multiple back plane serial links are provided for input or output data as well as for off-card data storage.

Memory

The CHAMP-WB contains two wide 64-bit memory interfaces which use fast DDR3L memory. Each bank is 4 GB with a potential future upgrade path to 8 GB. Running at a minimum of 600 MHz DDR, the two memory banks provide at least 9.6 GB/s of peak memory bandwidth per bank. Full thermal characterization will determine the final supported speed. Note that due to SDRAM latency, actual throughput is very dependent on data block transfer size. The larger the data blocks, the closer to the theoretical maximum throughput can be achieved as inter-block gaps are minimized.

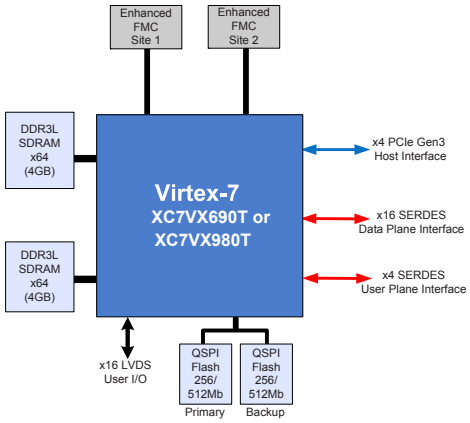

Figure 3: FPGA Memory & I/O

FPGA backplane I/O

The FPGA node on the CHAMP-WB has multiple back-plane SerDes that can be used for different functions.

One of the x4 GTH SerDes links is dedicated to a Gen3 x4 PCIe link which is connected to a Gen3 PCIe switch. This path is generally used as the host interface into the FPGA and is connected to the PCIe expansion plane on the backplane and can be controlled by any processor board that has a PCIe link to the expansion plane such as the VPX6-1957 or CHAMP-AV8.

Note that an OpenVPX chassis which supports the expansion plane on P2 is recommended to support this host path. This path could also be used for the FPGA to transmit data, but that is not the generally supported use-case.

16 other GTH SerDes links are connected to the 16 data plane signals on the backplane P1 connector. Because these signals are directly connected to the FPGA they can support any protocol, depending on what FPGA IP core is implemented inside the FPGA. The initial configuration will be to support Gen2 SRIO or Aurora, but other options such as 10 GbE are also possible. These SerDes can run up to 10.3 Gbps.

Note that while PCIe can be supported with a PCIe core inside the FPGA, it requires a build variant as the line termination is different than the other protocols. The remaining x4 GTH SerDes link is connected to the P4 connector on the backplane as part of the User Plane I/O. This link can also run up to 10.3 Gbps.

The backplane SerDes all have access to a fixed 312.5 MHz oscillator and a SiLabs SI570 Programmable clock. Combining these different potential reference clocks with the configurable multiply/divide settings for each quad-SerDes provides maximum flexibility for potential line rates. Configuration of the programmable clock can be done through the V7 FPGA via an I2C interface.

The Virtex-7 has Xilinx's latest generation 2D eye scan capability that enables visibility right at the SerDes receiver. The observation point is also after equalization so that the effects of equalization can also be seen. Xilinx now has an RX Margin Analysis tool which can characterize the receive channel. Control for the SerDes are also accessible in the reference design for customer tuning as needed. This extra controllability and visibility is essential when bringing up multi-gigabit signals on the backplane.

In addition to the SerDes links there are 16 LVDS pairs that go to the backplane, three of which are clock capable. There is also an additional clock capable pair that is dedicated as a 1 PPS clock signal.

FPGA Configuration

Two 256/512Mb QSPI Flash devices are connected to the FPGA for initial configuration. One of the devices is used to hold the default startup load, the other is a fallback image in case the primary image is corrupted. The FPGA and Flash can also be programmed directly with JTAG. Using Tandem configuration it is also possible to program the FPGA directly via the PCIe bus from the host processor. More images can be stored with the host processor. Lastly the QSPI Flash can be programmed via software using a QSPI core inside the FPGA.

Configuration time will be dependent on FPGA option, whether or not compression is used and whether or not the image is encrypted. The worst case is the X980T FPGA with no compression and encryption which can take about 1.5 seconds assuming a 100 MHz configuration clock. Without encryption, but no compression, configuration time will be about 600 ms for the X690T and about 720 ms for the X980T device. Compression can cut these times significantly. Alternate configuration clock frequencies will also affect these times.

Encrypted bit files are supported and either the eFUSE key or volatile key can be used. Power needs to be maintained on the backplane VBAT pin in order to maintain the volatile key if power is removed from the board.

Host Interface

The CHAMP-WB does not have a processor on card. Instead it is architected to have a separate processor card such as the VPX6-1957 or CHAMP-AV8 card control 1 to 4 of the CHAMP-WB cards. The PCIe host interface of the FPGA is connected to a Gen3 PCIe switch which has two x8 connections to the expansion plane on P2 backplane connector. Using an OpenVPX chassis with the expansion plane routed, a single processor card in one slot can control multiple CHAMP-WB cards through the daisy-chained expansion plane. PCIe MSI packets are used to send interrupt information back to the host processor.

Using this same mechanism the CHAMP-FX4 can also control the CHAMP-WB-DRFM by running the driver on the dual ARM Cortex A9 processor inside the ZYNQ® All Programmable SOC. Connectivity needs to be provided between the FX4 PCIe switch and the CHAMP-WB-DRFM PCIe switch.

The FPGA is also directly connected to the Data Plane on P1 backplane VPX connector. The data plane is usually used for the FPGA to transmit processed sensor data on to the general purpose processor. DMA engines inside the FPGA are used to provide this function and are controlled by the host processor via descriptor chains.

Note: The CHAMP-WB can also be used with Curtiss-Wright's latest 40G products by using either the PCIe switch or the backplane SerDes as PCIe for data transfers to the 40G fabric via the VPX6-1958 or CHAMP-AV9.

Figure 4 shows the backplane connectivity for the module.

Board connectivity OpenVPX backplane data plane

The default data plane option is Gen2 SRIO which can be used to connect to any other card which supports SRIO. An SRIO endpoint is implemented inside the FPGA and provides data-plane connectivity on the back plane. The standard reference design implements a single x4 Gen2 SRIO endpoint connected to the first set of x4 links on the backplane. These can be moved or replicated to the other links as needed. In addition a DMA engine is provided with in-band doorbell generation support to manage transfer of processed data to a remote processor for post processing. SRIO is used when communicating with the VPX6-1957 or the CHAMP-AV8. The VPX6-6902 SRIO switch can also be used to provide an external SRIO switching capability if a large number of SRIO endpoints will be in the system.

Note that only 5.0 GHz Gen 2.1 SRIO is supported.

When communicating with other FPGA cards, it is easier to provide Aurora interconnectivity between the FPGAs as Aurora has less overhead, supports faster rates, and consumes less internal resources. DMA IP is provided along with support for Aurora to facilitate this interconnectivity.

Other protocols such as PCIe or 40GbE can be supported with appropriate cores inside the FPGA. Note that PCIe requires a build option to change the AC blocking caps.

PCI Express (expansion plane)

As mentioned in the Host Interface section, the PCIe switch is used for the host processor to control multiple CHAMP-WB cards. This interface can also be used to transmit data out to a host processor or pulled out by a GPGPU.

Cabling

Since the CHAMP-WB is controlled by an external host processor. Most standard interfaces like serial ports and Ethernet will be interfaced to via the SBC or DSP card which is managing the CHAMP-WB. There is a JTAG connector and a reset button on the front panel of the CHAMP-WB. It is critical that the chassis being used provided connectivity via the P2 expansion plane between the host card and CHAMP-WB or that this connectivity can be provided externally via cables.

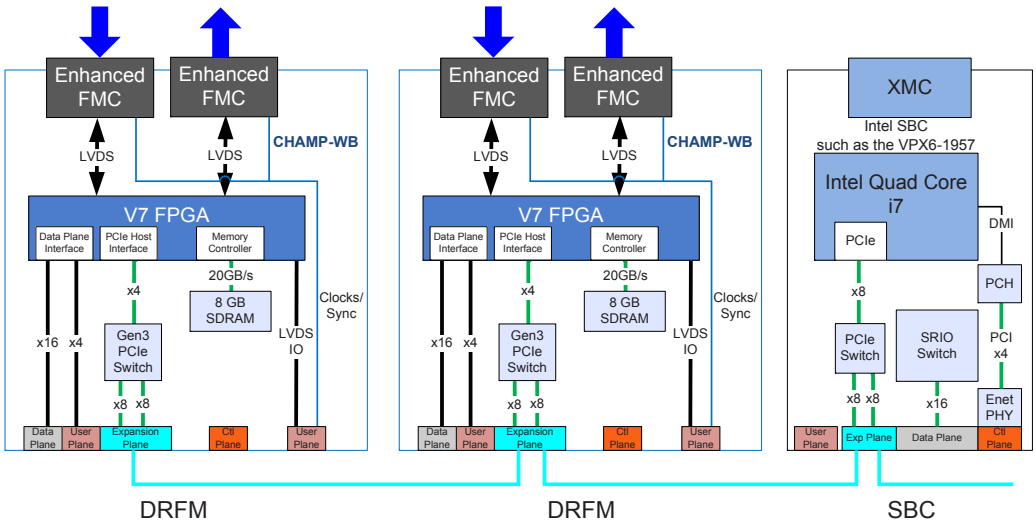

Figure 4: Diagram of 1957 with two CHAMP-WBs

A Rear Transition Module is available for additional access to some of the backplane signals. See the RTM section for more details.

Meritec also provides a large selection of different types of VPX compatible cables/connectors for additional back plane connectivity.

Chassis Management

An onboard CPLD controls chassis management and other general board support functions. The CPLD is connected to the Virtex-7 FPGA via an I2C interface and can be accessed by the host processor. Through the CPLD, LED, jumper, geographical address and other configuration information can be accessed. The Virtex-7 FPGA also has an I2C interface which is connected to temperature and backplane current monitors. The host processor can access this interface also for temperature and current monitoring. The CPLD is also connected to the backplane SM bus for some base IPMI support. The CPLD is power with 3.3V AUX so that it remains powered if the other supplies are turned off and 3.3V Aux remains powered. Logic is included to enable the CHAMP-WB to be powered on or off remotely via this path. The CPLD is also used to maintain the status of the red FAIL_LED when the main power is disconnected for 'persistent FAIL LED' support.

VITA 67.2 Support

In the standard configuration the P6 connector is not used and not populated. However the footprint for the P6 connector supports the option to populate a VITA 67.2 connector. Using this option, RF signals can be routed to a backplane RF connector and connected to the mezzanine sites on card. This provides an alternative option for routing RF signals to the mezzanine sites without having to utilize the front panel. Up to eight signals are supported on this connector. See the figure below for a view of the connector populated along with the other standard VPX connectors.

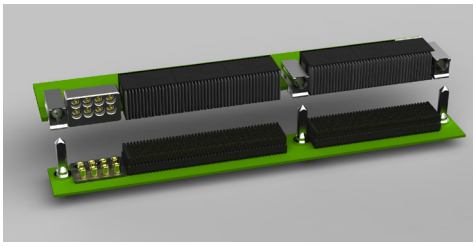

Figure 5: VITA 67.2 connector

Mezzanine Sites

The CHAMP-WB includes a versatile set of I/O options through dual enhanced FMC sites. The dual enhanced FMC sites provide flexibility for the latest I/O such as A/D converters, sFPDP, LVDS, and Fibre Channel, but also allows support for legacy I/Os. The sites are called enhanced FMC sites because not only do they support standard FMCs but an extra connector has been added to each site in order to be able to support additional I/O bandwidth.

The extra connector provides at least another 48 LVDS pairs, an SPI interface, additional power supply signals along with additional clock and sync signals from the back plane. Further details are listed below.

Both mezzanine sites are connected to the single Virtex-7 FPGA providing the optimal platform for DRFM or other sense-and-response applications.

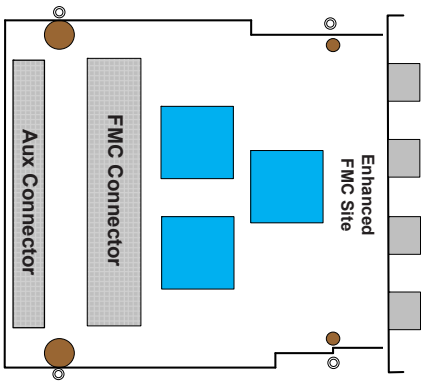

Figure 6: Mezzanine I/O support

FMC site

The VITA 57 FPGA Mezzanine Card (FMC) sites utilize two sets of160 user I/O pins (routed as 80 differential pairs) from the V7 FPGA:

- LA[00-33]_P/N = 34 differential pairs/68 single-ended with DCI termination
- HA[00-23]_P/N = 24 differential pairs/48 single-ended with DCI termination
- HB[00-21]_P/N = 22 differential pairs/44 single-ended with DCI termination
- DP[0-7]_M2C/C2M_P/N = 8 bidirection highspeed SerDes connections are available on site 2 as a build option. (note that to support this build option x8 lanes that are normally routed to the backplane are routed to this connector.) This option is not available on site 1.

Customer developed, third party, or Curtiss-Wright FMC modules can be used with the CHAMP-WB. Announced FMC products from Curtiss-Wright, such as the FMC-516/518 include analog I/O boards which can be used to tailor the I/O capabilities of the CHAMP-WB to customer project specific needs.

IMPORTANT NOTE: Unlike previous Xilinx devices, the Virtex-7 does not support 2.5V I/O. Therefore any FMC used on the CHAMP-WB cannot drive or require 2.5V signaling. The Virtex-7 can drive LVDS compatible signals with 1.8V supply, so the CHAMP-WB FMC banks do support LVDS that are on most FMCs. However no signals can exceed 1.8V. Most recent FMCs are 1.8V compatible.

Using the CHAMP-WB along with Curtiss-Wright's Signal Acquisition FMC cards such as the FMC-516/FMC-520 provides a complete Digital RF Memory Solution utilizing a quad channel 250 MS/s 16-bit ADC and a quad channel 250 MS/s 16-b DAC. Since FMCs have no FPGA on them and are lower power, they are better able to handle extreme rugged conditions. Furthermore with the flexibility of the FMC interface, alternate front ends can be accommodated by using different FMC modules

Enhanced FMC site

In addition to the standard FMC sites, the CHAMP-WB also has a secondary connector behind the FMC connector for additional I/O support. This auxiliary connector provides an additional 48 LVDS pairs for each site as well as some other enhanced capability.

Each additional connector contains the following signals:

1) 48 differential pairs (LVDS normally)

   a. Note that if the X980T part is used, two I/O banks are removed from that device which results in only 32 pairs being available on site 1.

   b. If the X690T part is used an additional 12 differential pairs are available on site 1, bring the total LVDS pairs available on site 1 enhanced FMC connector to 60 LVDS pairs

2) SPI interface

3) Backplane LVDS clock signal

   a. This clock is nominally a 10 MHz or 100 MHz clock which is distributed on length matched nets to both auxiliary connectors and the FPGA. Optionally, a local 100 MHz oscillator can also be used instead of the backplane clock.

4) Backplane SYNC/Clock signal

   a. This is another LVDS signal which is driven through low skew buffer to both auxiliary connectors and the FPGA.

Contact Curtiss-Wright for more information about secondary connector and the format of the larger mezzanine option.

FMC (VITA 57)

Traditional open standard bus-based structures like PCI-X are less suitable for FPGA I/O, because they can slow data transfer rates while consuming valuable FPGA resources. FPGA I/O is inherently configurable and can be adapted to a wide range of I/O structures. FPGA I/O is best optimized when FPGAs are not treated the same way as CPUs, rather are connected directly with I/O devices or ports. The VITA 57 FMC open standard has been developed to capitalize on these FPGA attributes.

The FMC standard provides an industry standard mezzanine form factor in support of a flexible, modular I/O interface to an FPGA located on a baseboard or carrier card. It allows the physical I/O, interface to be physically separated from the FPGA design while maintaining a close coupling between a physical I/O interface and an FPGA through a single connector, P1.

There is a choice of two very high-bandwidth connectors to interface the FMC to an FPGA on a carrier: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. An FMC with the LPC connector can mate with a carrier that utilizes either an LPC or HPC connector.

The use of the FMC standard simplifies FPGA designs, reduces cost, and makes the design of I/O mezzanine modules simple and straightforward. Development cycles can be shortened and costs lowered by utilizing a single FPGA design in multiple applications, by simply mounting different FMC modules.

Typical FMC modules will have an I/O device, such as an ADC (with front end signal conditioning), buffer and connectors. Since FPGAs can interface directly to I/O device pins, there is no need for any bus interfaces like PCI. Therefore bus converters are unnecessary overhead that can be left out of the design.

FMCs can be used to provide analog I/O, digital I/O, fiber-optic interfaces, camera interfaces, frame grabbers, additional memory or even dedicated DSP functions.

FMC modules are of a similar width, but half the size of PMC or XMC modules, but provide higher density host I/O.

Key FMC features include:

- 80 differential I/O pairs
- 10 high-speed serial I/O links (max of 8 supported on each site on FX4)
- Air and conduction-cooled variants
- Module size of 69 x 76.5 mm

Software and HDL

Software driver

The CHAMP-WB can be delivered with either Wind River VxWorks or Fedora Linux Drivers. The driver is installed on the host card and contains the necessary drivers for enumerating and enabling all onboard hardware devices, such as memories, SerDes, and the PCIe switch. The driver contains all the functions necessary for configuring the FPGAs, configuring the board logic, retrieving board status, managing DMAs and handling interrupts. The driver also has a function for remotely powering on/off the card through the backplane I2C interface.

FPGA Development kit

The FPGA Development kit provides FPGA HDL functions, application APIs, drivers, and utilities to simplify the task of integrating FPGAs into an embedded real-time DSP system design. It aids customers in the development of their FPGA algorithms and logic for Curtiss-Wright customer-programmable FPGA products. All the building blocks are provided to build a fully functional FPGA design into which a customer can integrate their FPGA logic and algorithms. It provides mechanisms for communication between FPGAs as well as communication between FPGAs and processors. Also included in the Kit is an example design that shows how to implement common FPGA functions such as control registers, DMA engines and interrupts, and how to control these functions and communicate with them from software. The FX Toolkit is comprised of a Hardware Development Kit (HDK) and Software Library.

The FPGA HDK contains HDL functions that are common to most FPGA application, such as DDR3L. There are HDL functions provided such as DDR3L memory controllers, RocketIO interfaces, parallel I/O interfaces. Commonly used FPGA functions are included, such as DMA engines and register sets. In addition, cores are supplied with the toolkit to support a Gen3 PCIe endpoint and a complete Gen2 SRIO core with DMA and doorbell generation capability. Options are provided to remove unneeded cores that may not be required for a particular design.

FusionXF based IP, such as cores used to support Curtiss-Wright FMCs are also supported within a reserved address space.

Rear Transition Module (RTM)

The purpose of the CHAMP-WB RTM is to provide access to backplane signals that are not routed in the backplane itself. If signals such as data-plane signals are routed in the backplane they are not connected to the RTM as those connections would create stubs and impact signal integrity.

- The following signals have access from the front panel of the RTM:
  - All SerDes connections(data plane, PCIe expansion plane, User Plane RocketIO) that are not routed in the backplane can be accessed with iPASS-HD cables. (CBL-474-iPASSHD)
  - All signals available through high density connector/ cable (CBL-474-FPL-000)
  - JTAG, reset, diagnostics (RS232, Ethernet signals if future variant with processor)
  - BP_Clock – Differential LVDS clock (SMA)
  - BP_SYNC – Sync signal (SMA)
- The following signals have access from the top-side of the RTM:
  - LVDS DIO, Jumpers

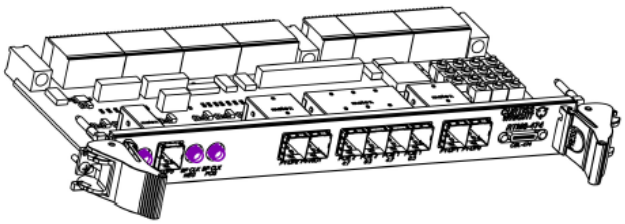

Figure 7: Line drawing of Rear Transition Module (RTM)

Ordering Information

Check with a Curtiss-Wright representative for availability of specific part numbers.

TABLE 3 Ordering information - VPX6 - 474 - UVWXabc[-E]

PART NUMBER	AVAILABLE OPTIONS	
Standard prefix for 6U VPX cards	VPX6	
Model number	474	
U: Cooling method	A: Air-cooling C: Conduction-cooling	
V: Temperature range	0: 0 to 50°C 1: -40 to 71°C 2: -40 to 85°C (conduction-cooled only) contact factory	
W: Mechanical format	4: 1” pitch, no 2-level maintenance support 5: 1” pitch, 2-level maintenance support (covers)	
X: FPGA or cardset type	Base card only variants (X = numeric value) 0 or 1 = X690T -2 2 = X980T -2 (0 to 50°C only) 3 = X690T -3 (0 to 50°C only)	Card set variants A = ADC only D = DAC only T = Transceiver (ADC and DAC)
Build options	Base card only variants (X = numeric value) a: SerDes 0 = all to backplane (non PCIe) 1 = 8 x routed to FMC site 2 2 = all to backplane (PCIe) b: P6 0 = not populated 1 = VITA 67.2 connector c: Mezzanine connectors 0 = FMC and AUX connectors populated 2 = SFP/QSFP compatible	Card set variants (X = A, D, or T) a: Mezzanine number 0 = TADF-430x (12 GS/s ADC/DAC) b: FPGA/speed grade 0 or 1 = X690T -2 2 = X980T -2 (0-50°C only) 3 = X690T -3 (0-50°C only) c: Reserved
[-E]	-E: to be added to indicate EAU models	