GTS/DEC/004

Smart Source Selector and PCM decommutator PCI board (20Mbps) - 2ch

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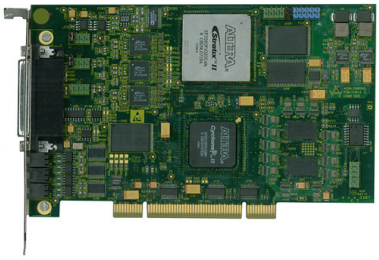

Key Features

- Bit error rate performance within 1dB of theory
- Bit-rates up to 20Mbps (NRZ-L codes)
- Uses signal quality estimates to weigh input signals
- Yields performance gain of up to 3dB when all channels are used
- NRZ-L/M/S, BIØ-L, derandomizer (11,13,15,17, 23)
- Sync word length up to 64 bits
- 0 to 16 bits sync word error tolerance
- 4 to 64 bits per word
- Supports digital IRIG-B 000, 001, 002, 003 time formats

Applications

- Real-time ground stations
- Telemetry data links

Overview

The GTS/DEC/004 reconstructs a serial PCM data stream from a source that has been corrupted by noise, phase jitter, amplitude modulation, or base line variations. The all-digital design utilizes two independent, programmable matched filters and Phase Locked Loops (PLL) to track deviations in the bit-rate of the received signals.

The output from the bit synchronizers is fed into the Smart Source Selector thereby producing a hard decision (1 or 0) based on the signal quality of the received bits. If the soft values are shifted in time, data is re-aligned prior to combining the soft values.

The recovered data is then decommutated into frames. Each minor frame can be tagged with time from an IRIG-B source to an accuracy of 1µs.

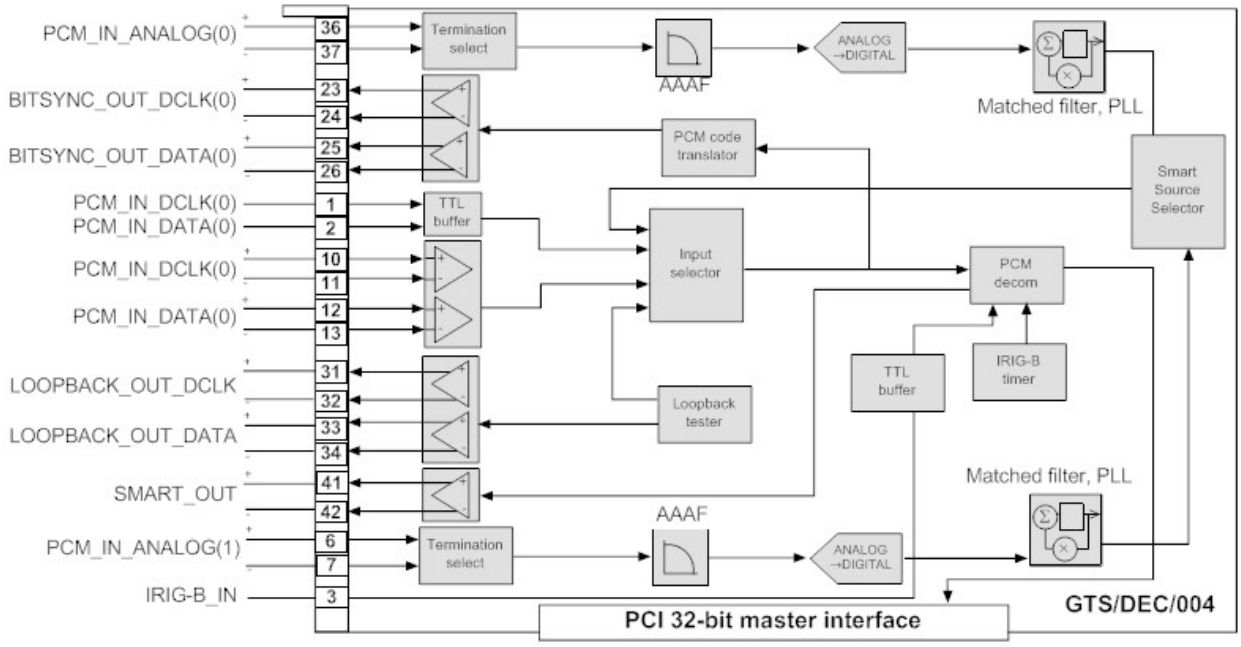

Figure 1: First of two bit synchronizers, Smart Source Selector and PCM decommutator channels

Specifications

All values provided in the following specification tables are valid within the operating temperature range specified under "Environmental ratings" in the "General specifications" table.

TABLE 1	General specifications				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Mass					
	–	142	–	g	
	–	5	–	oz	Design metric is grams.
PCI access rate	–	–	1,056	Mbps	
Power consumption					
total power	–	–	11	W	
Environmental ratings					
operating temperature	10	–	50	°C	
storage temperature	-25	–	70	°C	

TABLE 2	BTTL inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	3	–	
Signaling rate					
PCM_IN_DCLK(0)	–	–	20	Mbps	
PCM_IN_DATA(0)	–	–	20	Mbps	NRZ-L/M/S, RNRZ-L 11/13/15/17/23.
PCM_IN_DATA(0)	–	–	10	Mbps	BIØ-L.
IRIG-B_IN	–	–	1	Mbps	Digital IRIG-B 000, 001, 002, 003 time formats.
Input voltage					
operating range	0	–	5.5	V	
logic 0	–	–	0.8	V	
logic 1	2	–	–	V	
overvoltage protection	0	–	5.5	V	Voltages outside of this range can damage input.
Input resistance					
each input to GND	–	2.2	–	MΩ	Module powered on.
each input to GND	–	35	–	kΩ	Module powered off.

TABLE 3	RS-422 inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	2	–	
Signaling rate					
PCM_IN_DCLK(0)±	–	–	20	Mbps	
PCM_IN_DATA(0)±	–	–	20	Mbps	NRZ-L/M/S, RNRZ-L 11/13/15/17/23.
PCM_IN_DATA(0)±	–	–	10	Mbps	BIØ-L.

TABLE 3	RS-422 inputs (continued)				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Input voltage					
operating range	-7	–	12	V	Do not exceed operating range.
logic 0	–	–	-0.2	V	V_{IN+} - V_{IN-}.
logic 1	-0.01	–	–	V	V_{IN+} - V_{IN-}.
common mode voltage	-7	–	12	V	
overvoltage protection	-9	–	14	V	Voltages outside of this range can damage input.
ESD protection	–	16	–	kV	Human Body Model.
Input resistance					
between inputs	–	120	–	Ω	Module powered on and inputs terminated.
between inputs	–	120	–	Ω	Module powered off and inputs terminated.
each input to GND	–	5	–	MΩ	Module powered on.
each input to GND	–	69	–	kΩ	Module powered off.

TABLE 4	RS-422 outputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Outputs	–	–	5	–	
Signaling rate					
BITSYNC_OUT_DATA(0)±	–	–	20	Mbps	NRZ-L/M/S, RNRZ-L 11/13/15/17/23.
BITSYNC_OUT_DATA(0)±	–	–	10	Mbps	BIØ-L.
BITSYNC_OUT_DCLK(0)±	–	–	20	MHz	
LOOPBACK_OUT_DATA±	–	–	20	Mbps	NRZ-L/M/S, RNRZ-L 11/13/15/17/23.
LOOPBACK_OUT_DATA±	–	–	10	Mbps	BIØ-L.
LOOPBACK_OUT_DCLK±	–	–	20	MHz	
SMART_OUT±	–	–	–	–	For details, see “SMART_OUT output” on page 5.
Output voltage					
absolute operating range	-7	–	12	V	Absolute voltage of the operating signal must stay within this range.
logic 0	–	–	-3	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
logic 1	3	–	–	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
short circuit current	-250	–	250	mA	
short circuit duration	–	–	1	s	Only one output may be shorted at a time.
ESD protection	16	–	–	kV	Human Body Model.
Output resistance	–	50	–	Ω	

TABLE 5	Bit synchronizer inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	2	–	
Input signal amplitude					
PCM_IN_ANALOG(0)	0.3	–	20	V_{pp}	Peak-to-peak.
Input sources	–	–	–	–	Single ended or differential (selectable via jumpers).
Impedance	–	–	–	–	50Ω or 75Ω (selectable via jumpers).
Bit-rate					
NRZ-L/M/S, RNRZ-L 11/13/15/17/23	0.0128	–	20,000	kbps	
BIØ-L	0.064	–	10,000	kbps	
Maximum DC offset					
single ended	-5	–	5	V	
differential ended	-10	–	10	V	

TABLE 6	Bit synchronizer performance				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Loop bandwidth	0.01	–	2.0	%	
Offset bandwidth	–	100	–	%	
Gain bandwidth	–	100	–	%	
Acquisition range	0.04	–	5	%	
Tracking range	0.1	–	20	%	
Bit Error Rate	0.2	–	1	dB	Deviation from theory.
Sync maintenance	–	–	–	–	Retains sync with NRZ codes at EbNo = 3dB with 248 transition gaps every 1,024 bits.

TABLE 7	Smart Source Selector performance				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Match window size	0	60	64	Bits	
Worst case match time	–	–	1,200	Bits	

Setting up the GTS/DEC/004

The following tables list the setup configurations available for the GTS/DEC/004.

TABLE 8	Bit synchronizer settings	
SETTING	CHOICE	DEFAULT
Loop bandwidth [%]	0.01% to 2.0%	0.01%
Pulse shape	Rectangle Bessel Root Raised Cosine	Bessel

TABLE 9	Decommutator settings	
SETTING	CHOICE	DEFAULT
Input polarity	True False	True
Auto invert polarity	True False	False
Sync word mask	0 to 64	Based on size of sync word
Sync word error tolerance	0 to 16, but less than 25% of sync word bits	0
PCM clock phase [°]	0° / 90° / 180° / 270°	0°

TABLE 10	Smart Source Selector settings	
SETTING	CHOICE	DEFAULT
Match length	0 - 64	60

Getting the most of the GTS/DEC/004

NOTE: The GTS/DEC/004 is a half-length PCI-form board and is not currently verified for use in a PCI-X slot. Voltage levels are 3.3 or 5 volts. Dimensions are: W = 0.6 inches (15.24 mm) x D = 6.9 inches (175.26 mm) × H = 4.2 inches (106.68 mm).

GTS Software Development Kit (SDK)

The GTS SDK 3 includes APIs for system definition, programming and real-time data access, and documentation with detailed examples.

The GTS SDK 3 provides developers and system integrators with a toolkit for generating XidML® metadata files and programming the card. It also offers real-time access to decommutated data with time tags and status registers.

Bit synchronizer performance tuning

If offset modulation is affecting performance, adjust the offset bandwidth from 100% downwards to compensate. Likewise, if amplitude modulation is affecting performance, decrease the gain bandwidth.

Gain control bandwidth

This setting controls how quickly the automatic gain control responds to a change in amplitude; a higher setting (up to 100%) results in a slower filter response while a smaller setting (say 20%) results in a faster response.

Offset control bandwidth

This setting controls how quickly the automatic offset control responds to a change in offset; a higher setting (up to 100%) results in a slower filter response while a smaller setting (say 20%) results in a faster response.

Loop bandwidth filter

It is desirable to restrict loop bandwidth at higher bit rates. This is to prevent the PLL frequency from moving too far away from the PCM clock frequency and thereby introducing jitter.

Choosing fill words

Care must be taken when choosing fill words. For example, 0xAAAA (101010…..) or 0x5555 (010101…..) can result in loss of sync because 0xAAAA at 20Mb/s looks like 0xAAAA at 10Mb/s when using NRZ-M or NRZ-S. A fill word of, for example, 0x7E7E results in no loss of sync. By the same token, a fill word of 0xCCCC (11001100….) results in the same problem when using 20mb/s NRZ-L. Therefore, try to avoid repetitions of these types when choosing fill words.

Loopback tester

The GTS/DEC/004 features a loopback tester, which transmits a PCM frame to allow system checks. The loopback tester transmits frames as configured in the XidML setup. The loopback tester allows for dynamic and fixed data to be transmitted. The first eight parameters transmitted are dynamic counters that rollover to zero. The rest of the parameters are a fixed word (which is 0x1234). At present, the loopback tester only generates the minor frame layout as given in the configuration.

NOTE: The GTS/DEC/004 driver software is a minor frame decoder. Client software can use the SDK functions to decommutate major frames by adding minor frame tracking logic.

Status LEDs

The GTS/DEC/004 uses LEDs as shown in the following figure to indicate the current status of the card.

NOTE: The state of LEDs is undefined between power-on and the first driver access to the PCI card. Once the card is configured, behavior is as shown in the following table until the PC is powered off.

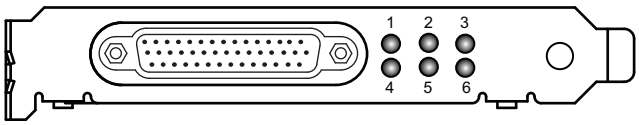

Figure 2: PCI card LEDs

TABLE 11 Status LED description

LED	NAME	DESCRIPTION
1	IRIG-B	Lights when the IRIG time signal is successfully received.
2	BS(0)	Lights solid green when the bit synchronizer is in lock with an incoming data stream on channel 0.
3	DECOM(0)	Lights solid green when the decommutator is in a lock state; when not lit the decommutator is in a loss, verify or check state.
4	PCI	Flashes green when the PCI card is operating correctly on the PCI bus.
5	BS(1)	Lights solid green when the bit synchronizer is in lock with an incoming data stream on channel 1.

TABLE 11	Status LED description	
LED	NAME	DESCRIPTION
6	SSS	Lights solid green when the Smart Source Selector is in a lock state and combining; when not lit, the aligner is not able to find the alignment point in the data.

J1 and J2 headers

The following figure shows the selection headers on the GTS/DEC/004 card. J1 is used for PCM_IN_ANALOG(0) and J2 is used for PCM_IN_ANALOG(1).

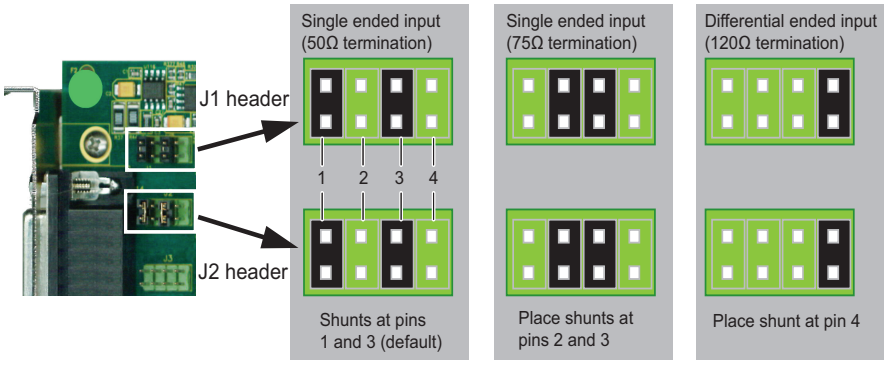

Figure 3: J1 and J2 selection headers

PINS	DESCRIPTION
1	Connects a 50Ω load between the + input and GND for single ended input (default).
2	Connects a 75Ω load between the + input and GND for single ended input.
3	Connects the - input to GND for single ended input (default).
4	Connects a 120Ω load between the + input and the - input for differential ended signals.

SMART_OUT output

The GTS/DEC/004 has a programmable output which can output one of the following signals when selected.

TABLE 12	Programmable output signals
SELECTED OUTPUT	DESCRIPTION
Minor frame pulse	High for last bit in sync word for at least 4 to 16 bits in frame (per decom channel).
Sync word found pulse	High for last bit in sync word location for at least 4 to 16 bits in frame (per decom channel).
Word pulse	High for last bit in word (per decom channel).
1 PPS pulse from IRIG_B time	Width of 1 PPS pulse is 16ns (high for 16ns every second).

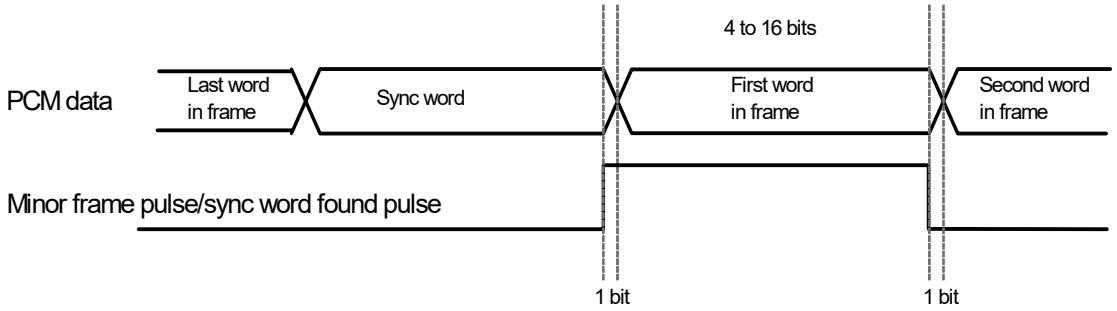

Figure 4: Minor frame pulse and sync word found pulse signals

When searching, the data rate is adjusted when the buffer is re-centred. This is reflected in the timestamp deviating from the true time until the buffer is re-centred.

Fill word patterns

Some fill word patterns when encoded, may contain repeating bit sequences, which can create a DC component. This DC component can then cause clock recovery to deteriorate. To avoid this deterioration, we recommend that the following patterns are used for fill words.

PCM code	Pattern
NRZ-L	AAAA or 5555
Bi-Phase-L	9669
NRZ-M or NRZ-S	0x7E7E or 0x3333 or 0xCCCC

Loop bandwidth settings

In general, set the loop bandwidth as tight as you can to avoid additional bit errors. For bit rates above 10Mbps, it is generally better to use a tighter bandwidth, whereas for bit rates below 10Mbps a more loose loop bandwidth can be set.

Maximum Stuck Bit Length

This setting is used to determine when a channel is considered *stuck* at 1 or 0 due to bad signal conditions. That is, the design allows a sequence for up to 48 (default) bits to be 1 or 0 without change before it declares the channel to be *stuck*. If you are using line codes, such as RNRZ-L or Bi-Phase-L, the setting never comes into effect since you always have transitions.

Glossary

TERM	DEFINITION
Sync word match tolerance	The number of bits (0-63) that can be incorrect and the sync word is still considered a match.
Matches to lock	The number of valid sync words (1-16) required after loss before the data is considered valid.
Misses to loss	The number of sync words (1-16) which fail the match tolerance before data is considered invalid.

Connector pinout of the GTS/DEC/004

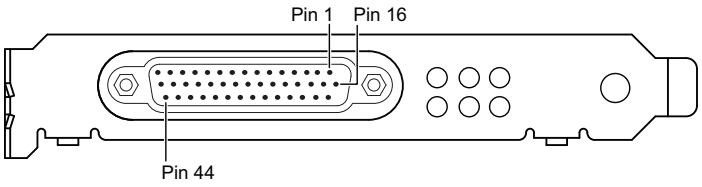

Figure 5: Connector pins

PIN	NAME	SEE SPECIFICATIONS TABLE	COMMENT
1	PCM_IN_DCLK(0)	BTTL inputs	PCM clock for channel 0
2	PCM_IN_DATA(0)	BTTL inputs	PCM data for channel 0
3	IRIG-B_IN	BTTL inputs	IRIG-B-002 input
4	DNC		Do not connect
5	GND	Internal ground	
6	PCM_IN_ANALOG(1)+	Bit synchronizer inputs	Differential ended bit synchronizer input for channel 1
7	PCM_IN_ANALOG(1)-	Bit synchronizer inputs	Differential ended bit synchronizer input for channel 1
8	DNC		Do not connect
9	DNC		Do not connect
10	PCM_IN_DCLK(0)+	RS-422 inputs	Differential ended PCM decommutator clock input for channel 0
11	PCM_IN_DCLK(0)-	RS-422 inputs	Differential ended PCM decommutator clock input for channel 0
12	PCM_IN_DATA(0)+	RS-422 inputs	Differential ended PCM decommutator data input for channel 0
13	PCM_IN_DATA(0)-	RS-422 inputs	Differential ended PCM decommutator data input for channel 0
14	DNC		Do not connect
15	DNC		Do not connect
16	GND	Internal ground	
17	GND	Internal ground	
18	DNC		Do not connect
19	DNC		Do not connect
20	GND	Internal ground	
21	DNC		Do not connect
22	GND	Internal ground	
23	BITSYNC_OUT_DCLK(0)+	RS-422 outputs	Differential ended bit synchronizer clock output for channel 0
24	BITSYNC_OUT_DCLK(0)-	RS-422 outputs	Differential ended bit synchronizer clock output for channel 0
25	BITSYNC_OUT_DATA(0)+	RS-422 outputs	Differential ended bit synchronizer data output for channel 0
26	BITSYNC_OUT_DATA(0)-	RS-422 outputs	Differential ended bit synchronizer data output for channel 0
27	DNC		Do not connect
28	DNC		Do not connect
29	DNC		Do not connect
30	DNC		Do not connect
31	LOOPBACK_OUT_DCLK+	RS-422 outputs	Differential ended loopback tester clock output
32	LOOPBACK_OUT_DCLK-	RS-422 outputs	Differential ended loopback tester clock output
33	LOOPBACK_OUT_DATA+	RS-422 outputs	Differential ended loopback tester data output
34	LOOPBACK_OUT_DATA-	RS-422 outputs	Differential ended loopback tester data output
35	GND	Internal ground	
36	PCM_IN_ANALOG(0)+	Bit synchronizer inputs	Differential ended bit synchronizer input for channel 0
37	PCM_IN_ANALOG(0)-	Bit synchronizer inputs	Differential ended bit synchronizer input for channel 0
38	GND	Internal ground	
39	DNC		Do not connect
40	DNC		Do not connect
41	SMART_OUT+	RS-422 outputs	Differential ended smart output (user configurable)
42	SMART_OUT-	RS-422 outputs	Differential ended smart output (user configurable)
43	DNC		Do not connect
44	DNC		Do not connect

Ordering information

PART NUMBER	DESCRIPTION
GTS/DEC/004/C	Smart Source Selector and PCM decommutator PCI board (20Mbps) - 2ch

By default, the standard cable, GTS/CON/002, is included with each card in the shipment. Its part number will be added to the Confirmation of Order unless an alternative option is specified (see the *Ground station cables* data sheet). The GTS SDK 3, software development kit for GTS-500 boards (SWP/SDK/003) is also included in the order. Additional items must be ordered separately; refer to Related products for options.

Revision history

REVISION	DIFFERENCES	STATUS
GTS/DEC/004/C	First release	Recommended for new programs

Supporting software

SOFTWARE	DETAILS
GTS SDK 3	Software development kit for GTS boards (XidML® 3.0)
DAS Studio 3	User interface for setup and management of data acquisition, network switches, recorders and ground stations in an integrated environment

Related products

MODULE	DETAILS
GS Works 9	Real-time and post-test data visualization and analysis software (Note, GTS/BSC/00x boards are not supported by GS Works 9 in standalone mode; they are only supported in conjunction with a PCM decoder such as a GTS/DEC/00x board.)

Related documentation

DOCUMENT	DETAILS
TEC/NOT/024	Evolution of Pulse Code Modulation
DOC/USG/016	Ground Station Boards User Guide
DOC/MAN/030	DAS Studio 3 User Manual