V3-152 Safety-Certifiable

Power Architecture QorIQ T2080 Single Board Computer

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Key Features

- NXP T2080 quad-core 64-bit CPU up to 1.8 GHz with AltiVec
- Up to 16 GB DDR3 memory
- x4 PCIe Gen2 XMC site
- Support for DDC-I Deos™, Green Hills Software INTEGRITY® tuMP™, Linux®, Lynx Software Technologies® LynxOS®, SYSGO® PikeOS®, U-Boot, and Wind River® VxWorks® 7 and VxWorks® 653
- NXP Secure Boot

Applications

- Commercial
- Control Computers
- Mission Computers
- Controllers
- ISR applications

Overview

Curtiss-Wright Defense Solutions' V3-152 is the DO-254 safety-certifiable variant of the VPX3-152, an OpenVPX™-compliant 3U single board computer (SBC) that combines the performance and the advanced I/O capabilities of the NXP® Power Architecture® QorIQ™ quad-core AltiVec™-enabled T2080 processor with an extensive I/O complement. Designed for space-constrained applications, the V3-152 represents the latest step in the evolution of commercial off-the-shelf (COTS) rugged, high-performance SBCs ideal for safety-certifiable and non-certifiable applications.

The challenge of high-density computing is to pack the greatest functionality into the smallest standard form factor, with the lowest power possible while retaining maximum flexibility. In conjunction with its processing power, the V3-152 easily meets this challenge by offering an impressive complement of I/O capability in order to satisfy the most demanding application needs with a low power footprint. For applications that demand the highest levels of hardware and software protection, the V3-152 provides information assurance with NXP Secure Boot technologies and capabilities.

The V3-152's integral high-speed backplane and XMC connectivity allow for multi-GBps data flows from board-to-board through the backplane interface and from the backplane to XMC site. This supports the acquisition, processing, and distribution of sensor data such as video, radar, and sonar data. The V3-152's rich I/O complement includes up to four Gigabit Ethernet (GbE) ports, four serial channels, up to 4 bits of LVTTL discrete digital I/O (DIO) inputs and up to 4 bits of LVTTL outputs, and an XMC site with 64 bits of I/O mapped to the backplane.

The V3-152 is supported by non-certifiable operating systems, such as Curtiss-Wright developed U-Boot, Linux, and Wind River VxWorks 7. As well, the board is supported by DO-178 certifiable operating systems through a Curtiss-Wright and MANNARINO developed VxWorks 653 BSP, as well as BSPs from our partners: DDC-I, Green Hills Software, Lynx Software Technologies, and SYSGO.

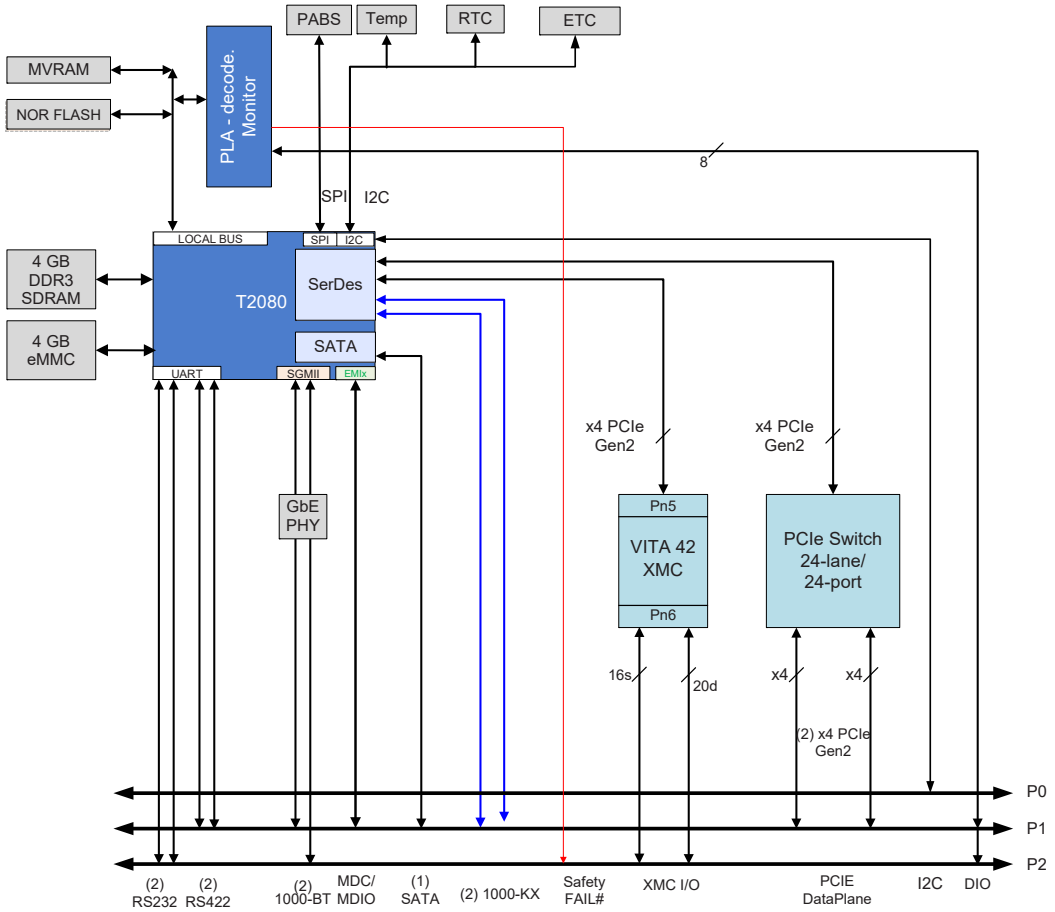

Figure 1: V3-152 block diagram

Features

- NXP QorIQ T2080 up to 1.8 GHz
  - 4 x dual threaded e6500 processor cores
  - Each core has AltiVec vector processor
  - Each core has 64 KB L1 cache
  - Shared 2 MB L2 cache
  - 1 x DDR3 memory controllers with 512 KB L3 front side cache ECC
  - 2 x GbE controllers
  - 2 x DUART controller
  - 2 x I2C channels
  - 3 x PCI Express® (PCIe) interfaces
  - Integrated DMA controllers
- Single, high-speed 64-bit DDR3 SDRAM controller with ECC to correct single-bit errors and detect double-bit errors on single memory controller
- Up to 16 GB of DDR3 SDRAM with ECC
- 4 GB of SLC eMMC Flash (for other sizes, contact factory)
- 256 MB of contiguous direct-mapped Flash memory
  - Hardware Flash write protection jumper
- Permanent Alternate Boot Site (PABS) provides back-up boot capability
- 512 KB MRAM NVRAM
- PCIe fabric ports on the VPX P1 connector, mapped as per VITA 65, that can be configured as:
  - Four x2 lane PCIe Gen2 ports, transparent mode
  - Two x4 lane PCIe Gen2 ports, one non-transparent capable
  - Eight x1 lane PCIe Gen2 ports, two non-transparent capable (other configurations possible, consult factory)
- 1 x XMC (VITA 42.3) site on independent PCIe bus
  - x4 lane PCIe Gen2 interface
  - PN6 pinned out to backplane P2 following VITA 46.9 P2w1-X16s+X8d+X12d
- Conduction-cooling of XMC site optimized with primary and secondary thermal interfaces

- Two 1000BASE-T GbE interfaces on P1 and P2 connector mapped
- Two 1000BASE-KX also configurable as 10GBASE-KR on P1 connector as per VITA 65
- Two 1000BASE-T Ethernet also configurable as 1000BASE-BX
- Up to two SATA 2.0 ports
- 2 x asynchronous EIA/TIA -232 serial ports
- 2 x asynchronous EIA/TIA -422 serial channels
  - + Configurable as EIA/TIA -232
- 4 x 5V-tolerant LVTTL DIO inputs, with interrupt capability
- 3 x 5V LVTTL DIO outputs
- General purpose DMA controllers provided by the T2080
- 2 x avionics-style (windowed) watchdog timers with external watchdog event indicator provided by the Safety Monitor PLD
- 2 x on-board temperature sensors with alarm interrupt plus a processor temperature sensor
- Elapsed Time Counter (ETC) to record the total power-on time across product's life span
- Status LEDs
- +5V operation
- Curtiss-Wright's U-Boot firmware providing a comprehensive suite of system debug, exerciser, and update functions, plus BIT and non-volatile memory sanitization function
  - + For safety-certifiable variants, a certifiable boot loader can be provided (contact RTOS Partner)
- Circuit card assembly is lead-free as per Class 3 standards of IPC-A-610C, Acceptability of Electronic Assemblies
- Standard conformal coating is acrylic
- Available in a range of ruggedization levels
  - + Conduction-cooled Level 200 per VITA 46.0
  - + Conduction-cooled Level 300 per VITA 48.2, Type 1 card with top and bottom covers
- Available software packages
  - + VxWorks 653 3.0.1.1 BSP from Curtiss-Wright
  - + DO-178C BSPs available from software partners (DDC-I, Green Hills, Lynx Software and SYSGO)

Table 1 below compares the key characteristics of the T2080-based V3-152 SBC to those of the Arm-based V3-1703.

TABLE 1 V3-152 to V3-1703 product comparison

FEATURE	V3-152	V3-1703
Processing nodes	1	1
Processor	T2080 up to 1.8 GHz	LS1043A up to 1.6 GHz
Number of cores	4 x dual threaded e6500 cores with AltiVec	4 x A53 Arm 64bit cores with NEON SIMD
Memory banks	1 x, up to 16 GB (1 memory controller)	1 x, up to 8 GB (1 memory controller)
Memory bandwidth	Up to 1866 MT/sec	Up to 1600 MT/sec
I/O	2 x EIA-232, 2 x EIA-422, DIO, up to 4 GbE (2 x 1000BASE-T/BASE-X and 2 x 1000BASE-BX/KX), 1 x SATA 2.0	2 x EIA-232, 2 x EIA-422, DIO, 2 x GbE (1000BASE-T or 1000BASE-X), 1 x SATA 2.0 port
CPU data path (to switch)	x4 lane PCIe Gen2	x4 lane PCIe Gen2
Data plane	2 x4 lane ports (default). Other user-selectable configurations available	2 x4 lane ports (default). Other user-selectable configurations available
IPMI	No	No
I/O ROUTING		
XMC I/O	24 x single-ended + 20 x differential pairs (variant dependent). Current certifiable variant is 16s	24 x single-ended + 20 x differential pairs
XMC site	x4 lane PCIe G2 direct from T2080	x4 lane PCIe Gen2 thru PCIe switch, shared with backplane PCIe

Form Factor

VPX Module Format

The Versatile Performance Switching (VPX) module format, governed by the VITA 46 and VITA 65 specifications and the associated VITA 48 Ruggedized Enhanced Design Implementation (REDI), was established to address the fundamental requirement to provide open-architecture modules that incorporate high-speed serial interconnect technology that is becoming pervasive in high-performance computing. The VPX standard was developed by the leading providers of military COTS modules to address the major issue of high-speed serial interconnect, as well as incorporating numerous improvements learned after years of integrating VME and CompactPCI® (cPCI) modules. The VPX module format provides many benefits to integrators of high-performance multi-processor systems for radar, ISR, mission computers, and other applications. In short, the VPX standard provides:

- 3U and 6U Eurocard form factors that preserve chassis mechanical designs
- Support for various high-speed serial interfaces as the primary dataplane fabric
- Support for higher power modules and improved cooling
- Improved logistics with two-level maintenance and keying

Processor

NXP Power Architecture QorIQ

The V3-152 supports NXP's latest generation of QorIQ highly integrated system on chip processors, the quad core, 64-bit dual threaded T2080. The T2080 provides an extensive amount of I/O capability and processing power in a low power footprint, making it ideal for size, weight and power (SWaP)-sensitive applications.

The T2080 processor with four Power Architecture dual threaded 64-bit e6500 cores up to 1.8 GHz, each core with:

- 32 KBs L1 data cache with parity
- 32 KBs L1 instruction cache with parity
- 2 MB shared L2 cache with ECC
- 512 KB shared L3 cache
- AltiVec Vector engine

Airborne Safety Applications

The Airworthiness Regulator preferred approach for assuring that airborne hardware and software safely performs its intended function in its intended environment is to meet the RTCA/DO-254 and RTCA/DO-178 objectives applicable to the criticality of the function performed by the hardware/software. Criticality of a function is mapped to a Design Assurance Level (DAL) E though A, where E is the least critical and A is the most critical.

DO-254 and DO-178 objective compliance can be a costly and time-consuming undertaking, especially if the process is new to your organization. Over many years, Curtiss-Wright Defense Solutions has invested heavily in the people and infrastructure to efficiently deliver products capable of meeting the latest regulatory guidance provided by our design home country regulator, Transport Canada, as well as the FAA and EASA. Curtiss-Wright's breadth and depth of hardware and software design assurance experience has enabled us to produce re-usable design assurance artifacts for multiple safety-certifiable modules that will reduce your certification risk, project cost, and time to market.

The V3-152 is one of our state-of-the-art safety-certifiable modules that can be used to support functions with software and/or hardware DAL A requirements. Our certifiable COTS building block products can be modified to meet your unique hardware and software requirements, and Curtiss-Wright can provide the appropriate hardware and software lifecycle data to support your certification effort.

DO-254 Objective Compliance

Current guidance from the FAA provided in AC 20-152 recognizes the applicability of RTCA/DO-254 on complex custom micro-coded components (PLD and like devices) with hardware design assurance levels A, B, and C. In CM-SWCEH-001, EASA indicated for equipment and circuit board assemblies of DALs/IDALS A, B, C, or D that the DO-254 objectives of Appendix A defined for level D should be applied.

Curtiss-Wright's safety-certifiable circuit board assemblies, such as the V3-152, meet the objectives of DO-254 to DAL D. In addition, complex custom micro-coded components (such as the PLD on V3-152) meet the objectives of DO-254 to DAL A.

A Safety-Certifiable Artifact Kit can be ordered from Curtiss-Wright that contains a PHAC, HVP, Top-Level Drawing and HAS for the Circuit Board Assembly to support demonstration of DAL D objectives and a PHAC, HVP, Top-Level Drawing and HAS for the PLD to support demonstration of DAL A objectives. The remaining DO-254 lifecycle data is available for regulator or designate review if required.

Deliverables for Certification:

- Plan for Hardware Aspects of Certification, including Verification Plan
- Top-Level Drawing
- Hardware Accomplishment Summary

Support Documents for Certification (if requested by authorities):

- Hardware Design Plan
- Hardware Configuration Management Plan
- Hardware Requirements
- Hardware Design Data
- Assembly Drawings/Installation Control Drawings
- Hardware Traceability Data
- Hardware Review and Analysis Results
- Hardware Test Procedures
- Hardware Test Results

DO-178C Certifiability BSPs

The V3-152 software is designed using a development process that results in DO-178C DAL A certifiable software and supporting artifacts which are available from our software partners. Please contact sales for information on availability.

Memory

Double Data Rate (DDR3) SDRAM

The T2080 provides a single memory controller supporting DDR3 SDRAM, which the V3-152 uses to provide up to 16 GB DDR3 SDRAM. The DDR3 interface operates at a rate of 1866 MT/s for 4GB variants and 1600 MT/s for 8 and 16 GB variants.

To preserve data integrity, the V3-152 takes advantage of the processor's memory controller's ECC circuitry to correct single-bit errors and detect double-bit errors. The DDR is accessible from the processor, as well as the Ethernet and PCIe interfaces.

Flash Memory

The V3-152 is configured with 256 MB of NOR Flash Memory. The Flash will retain data for 20 years at +85°C. Note: these figures assume the sector the data is in has less than 1,000 erase cycles. The data retention drops as erase cycle count increases. After 10,000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year. Read performance of the Flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical.

For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable writing to Flash. The firmware provides Flash programming functions with support for downloading Flash images over Ethernet.

NAND Flash

For applications requiring more non-volatile memory storage than can be supported by the NOR Flash memory, the V3-152 provides 4 GB of SLC eMMC NAND flash. Other sizes will be available in the future (contact factory).

Permanent Alternate Boot Site (PABS)

The V3-152 is equipped with a Permanent Alternate Boot Site (PABS) SPI NOR Flash. PABS provides a backup boot capability in the event that the firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main Flash without removing the card from the system in which it is installed. An on-board jumper is provided to cause the card to boot from PABS, thus allowing a user to reinstall the standard firmware load.

MRAM NVRAM

An EVERSPIN MR20H50 Magnetoresistive Random-Access Memory (MRAM) provides 512 KB fast, non-volatile storage of mission data that must not be lost when power is removed. Data retention is greater than 20 years, with unlimited write endurance. Automatic data protection is provided on power loss.

Non-volatile Memory Security

The V3-152 provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices NOR and NAND Flash, NVRAM may be individually write-protected by a hardware jumper. The jumpers may be visually inspected to conform to security procedures.

The U-Boot firmware provides a non-volatile memory scrub function to perform a secure erase per NISPOM requirements.

The V3-152 I/O System

The V3-152 features a large number of I/O interfaces including EIA-232, EIA-422 serial, Ethernet, and LVTTL DIO. The details of the I/O interfaces are described in the following paragraphs.

Gigabit Ethernet Interfaces

The V3-152 provides two 10/100/1000BASE-T Ethernet interfaces, both implemented within the processor with an external PHY and transformers. One port is routed to P1 backplane connector and the other port to P2 backplane connector. The Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence. Depending on the configuration option ordered, the V3-152 can also support two 1000BASE-KX in addition to two 1000BASE-T Ethernets.

Fabric Ports

The V3-152 supports PCIe fabric ports to the backplane on P1 as per VITA 46 and VITA 65. Refer to Table 3 for the list of supported VITA 65 OpenVPX module profiles.

The backplane ports are connected from the processor to the backplane through a PCIe switch. The switch fans the processor downstream ports into the following configurations which are factory configured:

- Four x2 lane PCIe Gen2 ports, transparent mode
- Two x4 lane PCIe Gen2 ports, one non-transparent capable
- Eight x1 lane PCIe Gen2 ports, two non-transparent capable
- Other configurations possible. Consult factory.

Note that a PCIe Gen2 port is also capable of running at Gen1 speeds, hence these ports can be used to connect to other cards that are only Gen1 capable. Other configurations are also supported. Please consult the factory for any configurations not listed.

SATA

Depending on the variant, the V3-152 provides SATA 2.0 ports directly off the T2080 to the backplane.

Two EIA-232 Serial Ports

The V3-152 provides two EIA-232 serial channels. The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. One serial port supports a cable detect signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. Both ports utilize the processor's DUARTs. The Baud rate of both ports can be set independently from 300 to 115200 KBaud.

Two EIA-422 Serial Ports

The V3-152 provides two EIA-422 serial channels. Both of the serial ports support asynchronous communication with baud rates of 300 to 115200 in EIA-232 or 422 modes.

LVTTL Discrete DIO

The V3-152 provides 4x 5V-tolerant LVTTL DIO inputs, and 3x 5V-tolerant LVTTL DIO outputs. One DIO output is configured as Card_FAIL#. Each input DIO bit is capable of generating an interrupt upon a change of state, programmable to detect either edge. No protection is provided on DIO. See the user manual for more details.

Monitor

The V3-152 provides a variety of functions to monitor proper board function. The Monitor on the V3-152 includes an avionics watchdog timer, clock monitors, voltage monitors and temperature monitors. The monitor also serves as a decode of address space for Flash and non-volatile memory, and access DIO.

An external watchdog timer is provided and uses a single programmed time period, which defines a maximum interval between writes to the watchdog register.

Avionics (Windowed) Watchdog Timer

The watchdog timer is a pre-settable down-counter with a resolution of 1µsec. Time-out periods from 1 msec to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset, or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, the reset from a watchdog time out can be disabled. One of the four DIO can be configured as a watchdog event indicator signal, outputting to the backplane in the event of a watchdog timeout.

Extensive Timing Resources

The V3-152 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in the table below.

TABLE 2 V3-152 timing resources

TIMER	IMPLEMENTATION	TYPE	SIZE	TICK RATE/ PERIOD	MAXIMUM DURATION
PowerPC time base register	Four (one per physical core)	Free-running counter	64-bit	37.5 MHz/ 26.67 nsec	
PowerPC decrementer	Eight (one per thread)	Presettable, readable down counter	32-bit	37.5 MHz/ 26.67 nsec	114.5 sec
General purpose #0-7	T2080 MPIC	Presettable, readable down counter with auto-read and stop options, divide by 8, 16, 32 and 64	31-bit	37.5 MHz/ 26.67 nsec (default)	57.26 sec
RTC alarm	RTC	Alarm interrupt	-	1 Hz/ 1 sec	200 years
Watchdog timer	Monitor PLD	Presettable, readable down counterwith interrupt or reset on terminal count	25-bit	1 MHz/ 1 µsec	33.55 sec
Safety Watchdog	LTC6993 Timer Blox	Factory configured reset time	-	1 µsec	3 sec
Elapsed Time Counter	DS1682 Elapsed Timer Counter	Factory programmed total elapsed time recorder	32-bit	0.25 sec	34 years

General Purpose DMA Controllers

The processor provides three 8-channel DMA engines that are available for general purpose use. The DMA subsystem can be used for transferring blocks of data between the SDRAM, Flash memory, Gigabit Ethernet, and the PCIe interfaces. The DMA controllers support direct and descriptor-driven chained operation. The DMA controllers can support source and destination striding. The DMA controllers also feature a bandwidth management feature to allow the user to control the distribution of bandwidth between the DMA channels.

Elapsed Time Counter

The V3-152 provides an Elapsed Time Counter (ETC) device connected to the T2080's I2C bus to record the total power-on time across product's life span.

XMC Site

The V3-152 is equipped with one mezzanine site, capable of supporting VITA 42.3 XMC modules. The XMC site supports the VITA 46.9 X16s+X8d+X12d pin-out of 20 differential pairs and 16 single-ended signals. The XMC interface is a x4 lane PCIe Gen2 connection direct to the processor following the VITA 42.3 pinout. Additional single-ended I/O can be configured (contact factory for details).

XMC Specifications

- PCIe interface: 4-lane PCIe Gen2 as per VITA 42.3
- Pn6 I/O: 20 different pairs and 24 single-ended. Current certifiable variant is routed as VITA 46.9 P2w1-X16s+X8d+X12d.
- Differential routing: 100 Ohm differential, 50 Ohm for Pn6 I/O signals
- 3.3V power: Provided from backplane 3.3V (Vs2)
- VPWR power: Drawn from backplane 5.0V (Vs3)
- +/-12 V_{AUX}, 3.3V: Routed to XMC site but not used by card
- Maximum supported XMC power: 20W

XMC Power Routing

The XMC site is provided with 5V (Vs3), 3.3V (Vs2), +3.3V_{AUX}, +12V_{AUX}, and -12V_{AUX} power from the backplane as defined in VITA 46 for 3U basecards.

Conduction-cooled XMC Modules

To support the industry drive to open standards on conduction-cooled cards, the XMC site mechanical interfaces follow the VITA 20-2001 (R2005) conduction-cooled PCI Mezzanine Card (PMC) standard. To optimize the thermal transfer from XMC modules to the basecard, the standard V3-152 thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2005.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and the Curtiss-Wright TherMax™ thermal frame design provides optimum cooling for conduction-cooled XMC modules, allowing for higher power XMCs and/or increased long-term reliability through lower component temperatures.

Status Indicators and Controls

The V3-152 SBC provides fail status by illuminating a red front panel LED in the event the diagnostics detect a card failure. The SBC also provides a user-controllable, green front panel status LED.

COP Emulator Interfaces

The V3-152 provides access to the processor COP interface for on-chip debugging. Consult the Hardware User's Manual for more information if you need to use a COP emulator with the V3-152.

Temperature Sensors

The V3-152 provides temperature sensors to measure board and processor temperatures. There are two sensors to measure temperature on the card and one sensor to directly measure the die temperature of the processor using its thermal diode feature. The sensors can be read by software and may be configured to generate an interrupt in case of an over temperature condition.

Software Support

U-Boot Firmware and Monitor (not designed for use in safety-certifiable applications)

The monitor provides a command line interface over serial port to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

Built-in-Test (BIT) - a library of diagnostic routines to support Power-up BIT (PBIT) and Initiated BIT (IBIT) are designed to provide 95% fault coverage.

For safety-certifiable applications, a boot loader will be provided through partnership with associated OS vendors. Support for PBIT and IBIT should be discussed with selected OS vendor.

Operating System Software

- DO-178C-certifiable operating system support:
  - Deos certifiable BSP available from DDC-I
  - INTEGRITY-178 tuMP certifiable BSP available from Green Hills
  - LynxOS certifiable BSP available from Lynx Software Technologies
  - PikeOS certifiable BSP available from SYSGO
  - VxWorks 653 3.x Certifiable BSP to developed by Curtiss-Wright in partnership with Mannarino
- Non-certifiable operating system support:
  - 64-bit VxWorks 7.x from Curtiss-Wright
  - 64-bit NXP QorIQ Linux SDK v2.0 BSP from Curtiss-Wright

Rear Transition Module

To gain access to the backplane I/O signals of the V3-152, the RTM3-152 rear transition module (RTM) is available to access I/O in a lab environment. There are several variants of the RTM to match the V3-152 variants. Please contact the factory for more information.

Thermal Cooling

TherMax-style Thermal Frame

Applicable to conduction-cooled cards, a TherMax thermal frame provides an unbroken metallic path from the XMC sites and shunted components to the back-side cooling surface of the card, thereby minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB, which has a high thermal resistance compared to aluminum.

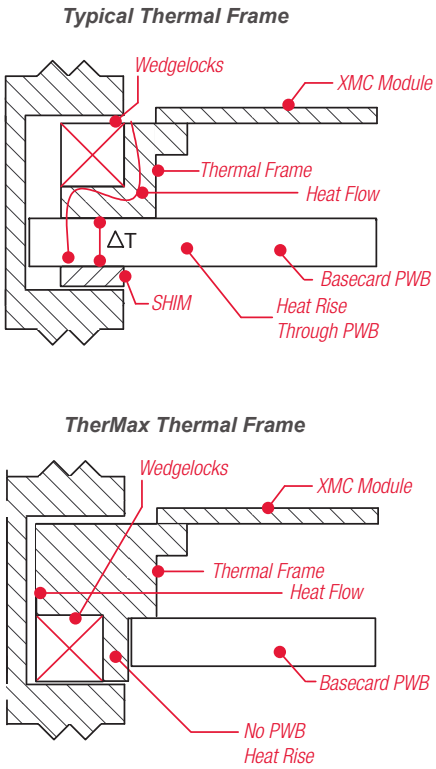

Figure 2: TherMax diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame

Full-width Thermal Interface to Back-side Slot Wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the V3-152, the thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 3. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long term reliability. During test and integration activities where it may be desirable to install a conduction-cooled V3-152 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

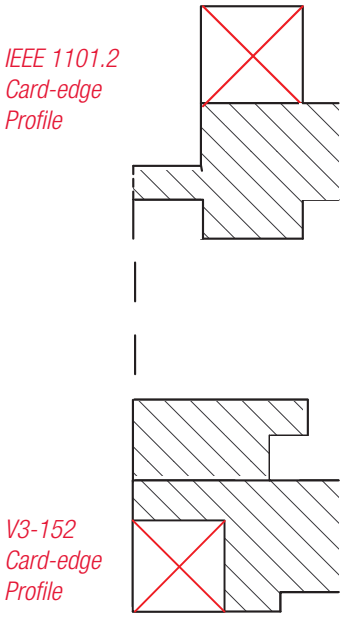

Figure 3: Card-edge profile deviates from IEEE 1101.2

V3-152 card-edge profile is optimized to provide a full-width thermal interface to the back-side slot wall

Specifications

Ruggedization Levels

- Air-cooled cards can be provided (contact factory).
- Conduction-cooled cards are available in Levels 200, 300.

Please see the Curtiss-Wright Ruggedization Guidelines product sheet for more information.

TABLE 3 Dimensions and weight

OPTION	DIMENSIONS	WEIGHT (grams)
Conduction-cooled L200	per VITA 46/IEEE 1101.1	463
Conduction-cooled L300 LRM	per VITA 48.2	535
RTM3-152	per VITA 46	164

Notes:

1. Refer to the deviation from IEEE 1101.2 in Figure 3.
2. Refer to Ruggedization Guidelines product sheet for more information.

TABLE 4 Power requirement

VOLTAGE	RUGGEDIZATION LEVEL	TYPICAL	TYPICAL MAX
5V (Vs3)	Level 200 Conduction-cooled	29.7W	35W
3.3V (Vs2)	Only routed to XMC		
+3.3VAUX	0.5W, and is routed to XMC site		
12V (Vs1)	Not used		
+/-12VAUX	Only used by XMC		

Notes:

1. Power estimates are for V3-152-C21A134C. No mezzanine installed.
2. All power rails defined as in VITA 46.0 for 3U basecards.

Ordering Information

The V3-152 is ordered with the following part numbers. V3-152-UVWXYPZ, where U, V, W, X, Y, P and Z denote cooling method, temperature range, mechanical format and functional configuration respectively. Not all possible configurations are offered, consult Curtiss-Wright for available configurations.

TABLE 5 Ordering information - V3-152-uvwxypzCtt

PART NUMBER	AVAILABLE OPTIONS
Model Number	V3-152
u: Cooling Method	Conduction-cooled
v: Ruggedization Level	1: L100 (-40 to 71°C) 2: L200 (-40 to 85°C) 3: L200 (-40 to 85°C) with 2-level maintenance covers 9: Customized Others: Reserved
w: Mechanical Format	1: 0.80” pitch 3: 0.85” pitch, with 2-level maintenance covers 5: 1” pitch, with or without 2-level maintenance covers 9: Customized Others: Reserved
x: Data Plane Mode / Certifiable Card	A: Two x 4 Gen 2 ports (software configurable) Four x 2 Gen 2 ports (software configurable) Eight x 1 Gen 2 ports with 2 NTB capable (software configurable) Others: Reserved
y: Control Plane Mode	1: 2x 1000BASE-KX Others: Reserved
p: Process/Memory Config	0: 1.5 GHz, 4 GB 1: 1.5 GHz, 8GB 2: 1.5 GHz, 16 GB 3: 1.8 GHz, 4 GB 4: 1.8 GHz, 8 GB 5: 1.8 GHz, 16 GB Others: Reserved
z: IO Mode	0: Reserved 1: 1x 1000BASE-T Ethernet, XMC with X24s+X8d+X12d, 1x SATA2, 2x EIA232, 2x EIA422, 4x DIO-in, 3x DIO out, Card_fail 2: Reserved 3: 2x 1000BASE-T Ethernet, XMC with X12s+X8d+X12d, 2x SATA2, 2x EIA232, 2x EIA422, 4x DIO-in, 3x DIO out, Card_fail 4: 2x 1000BASE-T Ethernet, XMC with X16s+X8d+X12d, 1x SATA2, 2x EIA232, 2x EIA422, 4x DIO-in, 3x DIO out, Card_fail Others: Reserved
C: Certifiable	Certifiable
tt: Customer Variant (if present)	Customer-specific number of certified base variant

Note:

1. V3-152-C21A134C is the current certifiable variant which has artifacts to support certification.
2. Not all combinations of an orderable variant are available as standard product. Variants highlighted in yellow are standard product.
3. Please consult your local sales office for further help in selecting the appropriate variant.
4. Conduction-cooled variants are delivered in a 0.8” pitch.

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