# VPX3-1703

## NXP Layerscape LS1043A Quad A53 Single Board Computer

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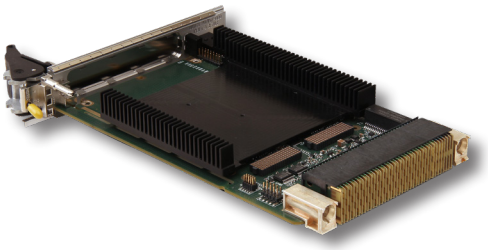

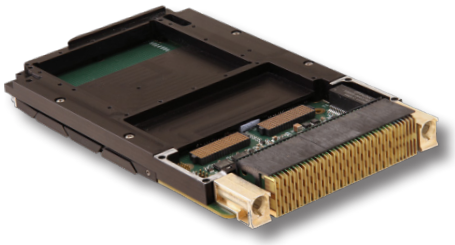

### Key Features

- NXP LS1043A Arm A53 quad-core 64-bit SOC up to 1.6 GHz
- 4 GB DDR4 memory
- x4 PCIe Gen2 XMC
- Curtiss-Wright's U-Boot, VxWorks 7, and Linux BSPs
- NXP Secure BOOT

### Applications

- Commercial
- Control Computers
- Mission Computers
- Controllers
- ISR applications

## Overview

Curtiss-Wright Defense Solutions' VPX3-1703 is the latest OpenVPX™-compliant 3U processor that combines the high performance of the NXP® Layerscape® LS1043A Arm® quad-core A53 processor with advanced I/O capabilities. Designed for space-constrained applications, the VPX3-1703 represents the latest step in the evolution of low-powered rugged Arm-based commercial off-the-shelf (COTS) SBCs.

### Arm processing

The challenge of high-density computing is to pack the greatest functionality into the smallest standard form factor, with the lowest power possible while retaining maximum flexibility. In conjunction with its processing power, the VPX3-1703 meets this challenge by offering an impressive complement of I/O capability in order to satisfy the most demanding application needs with a low power footprint. For applications requiring information assurance, the VPX3-1703 supports NXP's Secure Boot and trust capabilities.

The VPX3-1703's integral high speed backplane and XMC connectivity allow for multi-GB/s data flows from board to board through the backplane interface and from the backplane to XMC site supporting the acquisition, processing, and distribution of sensor data (such as video, radar, and sonar data). A rich I/O complement includes two Gigabit Ethernet (GbE) ports, four serial channels, up to four output LVTTL discrete digital IO (DIO), up to four input 5V tolerant LVTTL discrete DIO, Universal Serial Bus (USB) 2.0 or 3.0 ports (contact Curtiss-Wright for USB 3.0 support), and an XMC site with 64-bits of I/O mapped to the backplane.

The VPX3-1703 is supported by Curtiss-Wright's U-Boot, VxWorks®, and Linux® Board Support Package (BSP) and Driver Suites.

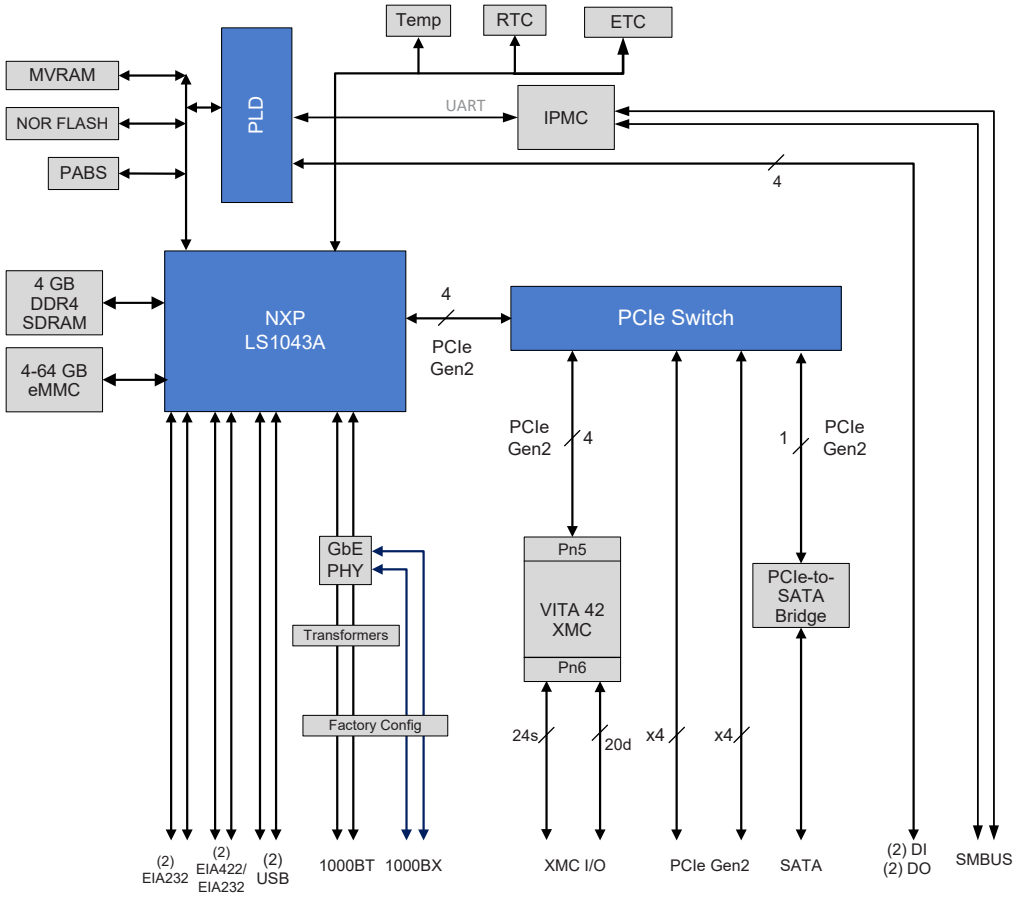


Figure 1: VPX3-1703 block diagram

# Features

- NXP LS1043A up to 1.6 GHz
  - 4 x A53 Arm processor cores
  - Each core has NEON SIMD processor
  - Each core has 32 KB L1 Instruction and 32 KB of L1 data cache
  - Shared 1 MB L2 Cache assignable to the 4 processing cores
  - 1 x 32-bit DDR4 memory controllers with ECC
  - 2 x GbE controllers
  - 2 x DUART controller
  - 3 x I2C channels
  - 3 x PCI Express® (PCIe) interfaces
  - Integrated DMA controllers
- Single independent high speed 32-bit (with ECC) DDR4 SDRAM controller with ECC to correct single-bit errors and detect double-bit errors on single memory controller
- 4 GB of DDR4 SDRAM with ECC
- Up to 64 GB of eMMC Flash (optional)
- 256 MB of contiguous direct-mapped Flash memory
  - Hardware Flash write protection jumper
- Permanent Alternate Boot Site (PABS) provides back-up boot capability
- 512 KB MRAM NVRAM
- PCIe fabric ports on the VPX P1 connector mapped as per VITA 65 that can be configured as:
  - Two x4 lane PCIe Gen2 ports, both non-transparent capable
  - Up to eight x1 lane PCIe Gen2 ports, two non-transparent capable
- 1 x XMC (VITA 42.3) site
  - x4 lane PCIe Gen2 interface
  - PN6 pinned out to backplane P2 following VITA 46.9 P2w1-X24s+X8d+X12d
- Conduction-cooling of XMC site optimized with primary and secondary thermal interfaces

- Two 1000BASE-T GbE interfaces on P1 connector mapped per VITA 65
  - Two 1000BASE-T also factory configurable as 1000BASE-X
- One SATA 2.0 port
- 2 x asynchronous EIA-232 serial ports
- 2 x asynchronous capable EIA-422 serial channels
  - Configurable as EIA-232
- Up to 4 output 5V tolerant LVTTL discrete DOs, and up to 4 input 5V tolerant LVTTL discrete DIs with interrupt capability
- 2 x USB 2.0 or 1 x USB 3.0 ports
- General purpose DMA controllers provided by the LS1043A
- 2 x avionics-style watchdog timers with external watchdog event indicator discrete, plus a fixed period period watchdog timer
- 2 x on-board temperature sensors with alarm interrupt, plus a processor temperature sensor
- IPMC controller or optional I2C port to backplane direct from LS1043A
- Status LEDs
- +5V operation
- Curtiss-Wright's U-Boot firmware providing a comprehensive suite of system debug, exerciser, and update functions, BIT, and non-volatile memory sanitization function
- Circuit card assembly is lead-free class 3 standards of IPC-A-610C, Acceptability of Electronic Assemblies
- Standard conformal coating is acrylic
- Available in a range of ruggedization levels
  - Air-cooled Level 0 and 100
  - Conduction-cooled Level 200 per VITA 46.0
  - Conduction-cooled Level 300 per VITA 48.2, Type 1 card with top and bottom covers
- Available software packages
  - 64-bit Linux BSP based on NXP SDK
  - 64-bit VxWorks 7 SMP BSP

Table 1 below compares the key characteristics of the Arm based VPX3-1703 to the T2080 based VPX3-152 SBC.

TABLE 1 VPX3-1703 to VPX3-152 product comparison

| FEATURE | VPX3-1703 | VPX3-152 |
|---|---|---|
| Processing nodes | 1 | 1 |
| Processor | LS1043A up to 1.6 GHz | T2080 up to 1.8 GHz |
| Number of cores | 4 x A53 Arm 64bit cores with NEON SIMD | 4 x dual threaded e6500 cores with AltiVec |
| Memory banks | 1 x 4 GB (1 memory controller) | 1 x, up to 16 GB (1 memory controller) |
| Memory bandwidth | 1600 MT/sec | Up to 1866 MT/sec |
| I/O | 2 x EIA-232, 2 x EIA-422, 2 x USB 2.0 or 1 x USB 3.0, DIO, 2 x GbE (1000BASE-T or 1000BASE-X), 1 x SATA 2.0 port optional | 2 x EIA-232, 2 x EIA-422, 2 x USB 2.0, DIO, up to 4 GbE (2 x 1000BASE-T/BASE-X and 2 x 1000BASE-BX/ KX/10GBASE-KR), 2 x SATA 2.0 |
| CPU data path (to switch) | x4 lane PCIe Gen2 | x4 lane PCIe Gen2 |
| Data plane | 2 x4 lane ports (default) Other user-selectable configurations available | 2 x4 lane ports (default) Other user-selectable configurations available |
| IPMI | Yes - variant dependent | Yes - variant dependent |
| I/O ROUTING | | |
| XMC I/O | 24 x single-ended + 20 x differential pairs | 12-24 x single-ended + 20 x differential pairs (variant dependent) |
| XMC site | x4 lane PCIe Gen2 thru PCIe switch, shared with backplane PCIe | x4 lane PCIe G2 direct from T2080 |

# Processor

## NXP Layerscape LS1043A

The VPX3-1703 supports NXP's latest generation of Layerscape highly integrated system on chip processors, the LS1043A quad core, 64-bit Arm A53 cores. The LS1043A provides an extensive amount of I/O capability and processing power in a low power footprint, making it ideal for size, weight and power (SWaP) sensitive applications.

NXP LS1043A processor with four Arm 64-bit A53 cores up to 1.6 GHz, each core with:

- 32 KBs L1 data cache with ECC
- 32 KBs L1 instruction cache with ECC
- 1 MB shared L2 cache with ECC
- NEON SIMD engine

# Memory

## Double Data Rate (DDR4) SDRAM

The LS0143A provides a single memory controller supporting DDR4 SDRAM which the VPX3-1703 uses to provide 4 GB DDR4 SDRAM. The DDR4 interface operates at a rate up to 1600 MT/s dependent on the processor speed.

To preserve data integrity, the VPX3-1703 takes advantage of the processor's memory controller's ECC circuitry to correct single-bit errors and detect double-bit errors. The SDRAM is accessible from the processor as well as the Ethernet and PCIe interfaces.

## Flash Memory

The VPX3-1703 is configured with 256 MB of NOR Flash Memory. The Flash will retain data for 20 years at +85°C. Note: these figures assume the sector the data is in has less than 1,000 erase cycles. The data retention drops as erase cycle count increases. After 10,000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year. Read performance of the Flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical.

For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable writing to Flash. The firmware provides Flash programming functions with support for downloading Flash images over Ethernet.

## NAND Flash

For applications requiring more non-volatile memory storage than can be supported by the NOR Flash memory, the VPX3-1703 can provide from 4 GB SLC up to 64 GB of MLC eMMC NAND flash.

## Permanent Alternate Boot Site (PABS)

The VPX3-1703 is equipped with a Permanent Alternate Boot Site (PABS) NOR Flash. PABS provides a backup boot capability in the event that the firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main Flash without removing the card from the system in which it is installed. An on-board jumper is provided to cause the card to boot from PABS, thus allowing a user to reinstall the standard firmware load.

## MRAM NVRAM

An EVERSPIN MR2A08A Magnetoresistive Random-Access Memory (MRAM) provides 512 KB fast, non-volatile storage of mission data that must not be lost when power is removed. Data retention is greater than 20 years, with unlimited write endurance. Automatic data protection is provided on power loss.

## Non-volatile memory security

The VPX3-1703 provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices NOR and NAND Flash, NVRAM may be individually write-protected by a hardware jumper. The jumpers may be visually inspected to conform to security procedures.

The U-Boot firmware provides a non-volatile memory scrub function to perform a secure erase per NISPOM requirements.

# The VPX3-1703 I/O System

The VPX3-1703 features a large number of I/O interfaces including EIA-232, EIA-422 serial, USB, Ethernet, SATA and LVTTL DIO. The details of the I/O interfaces are described in the following paragraphs. The VPX3-1703 is pin-out compatible with the VPX3-131, VPX3-133, and VPX3-152 (variant dependent).

## Gigabit Ethernet interfaces

The VPX3-1703 provides two 10/100/1000BASE-T Ethernet interfaces, both implemented within the processor with an external PHY and transformers. Both ports are routed to the P1 backplane connector and follow the pinout as defined by VITA 65. The Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence. Depending on the configuration option ordered, the two Ethernet ports can be factory configured as 1000BASE-X.

## Fabric ports

The VPX3-1703 supports PCIe fabric ports to the backplane on P1 as per VITA 46 and VITA 65. Refer to Table 5 for the list of supported VITA 65 OpenVPX module profiles.

The backplane ports are connected from the processor to the backplane through a PCIe switch. The switch fans the processor downstream ports into the following configurations which are user selectable:

- Two x4 lane PCIe Gen2 ports, both non-transparent capable
- Eight x1 lane PCIe Gen2 ports, two non-transparent capable

Note that a PCIe Gen2 port is also capable of running at Gen1 speeds, hence these ports can be used to connect to other cards that are only Gen1 capable. Other configurations are also supported. Please consult the factory for any configurations not listed.

## SATA

Depending on the variant, the VPX3-1703 has one SATA 2.0 ports to the backplane.

## Two EIA-232 serial ports

The VPX3-1703 provides two EIA-232 serial channels. The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. One serial port supports a cable detect signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. Both ports utilize the processor's DUARTs. The Baud rate of both ports can be set independently from 300 to 115200 Baud.

## Two EIA-422 serial ports

The VPX3-1703 provides two EIA-422 serial channels. Both of the serial ports support asynchronous communication with baud rates of 300 to 115200 in EIA-232 or 422 modes.

## LVTTL discrete DIO

The VPX3-1703 provides up to eight (8) LVTTL compatible DIO (max 4 input and 4 output), maximum (variant dependent). Each input bit is capable of generating an interrupt upon a change of state, programmable to detect either edge. No protection is provided on DIO. See user manual for more details.

## USB ports

The VPX3-1703 provides two USB 2.0 ports or one USB 3.0 port (factory configured) from the processor. Each USB 2.0 port can handle high speed (480 Mb/s), full speed (12 Mb/s), and low speed (1.5 Mb/s) operation. When operating at low speed or full speed, each port is managed by independent EHCI-compliant controllers internal to the device. One EHCI compliant controller manages any ports operating in high-speed mode. One USB port is accessible on the P1 connector and the other is accessible on the P2 connector. The 1703 provides a current limited +5V output to power external USB devices such as keyboards.

## Monitor

The VPX3-1703 provides a variety of functions to monitor proper board function. The Monitor on the VPX3-1703 includes a watchdog timer, clock monitors, voltage monitors and temperature monitors. The monitor also serves as a decode of address space for Flash and non-volatile memory, and access DIO.

The VPX3-1703 also includes an external watchdog timer which provides a single programmed time period, which defines a maximum interval between writes to the watchdog register. This watchdog runs on a clock independent to the processor clock.

## Avionic watchdog timers

The watchdog timer is a pre-settable down-counter with a resolution of 1 µsec. Time-out periods can be programmed up to 33.6 seconds. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, the reset from a watchdog time out can be disabled. One of the four DIO can be configured as a watchdog event indicator signal, outputting to the backplane in the event of a watchdog timeout.

## General purpose DMA controllers

The LS1043A supports enhanced Direct Memory Access (eDMA) through 32 independent DMA channels. DMA transfers are possible between system memories, General Purpose I/Os (GPIOs) and Slave Peripherals that support DMA.

In addition, the LS1043A supports a Queue Direct Memory Access Controller (qDMA). The qDMA is a high performance DMA and can be used for data transfers between DDR to DDR, DDR to PCIe for outbound transactions and DDR to memory-mapped flash interfaced through IFC. The blocks of data transferred can be represented in memory as contiguous or non-contiguous using scatter/gather table(s).

# XMC Site

The VPX3-1703 is equipped with one mezzanine site, capable of supporting VITA 42.3 XMC modules. The XMC site supports the VITA 46.9 X24s+X8d+X12d pin-out of 20 differential pairs and 24 single-ended signals. The XMC interface is a x4 lane PCIe Gen2 connection from the PCIe switch following the VITA 42.3 pinout.

## XMC power routing

The XMC site is provided with VPWR of 5V (from Vs3), 3.3V (from Vs2), +3.3V_ AUX, +12V_AUX, and -12V_AUX. These power rails come from the backplane as defined in VITA 46 for 3U base cards.

## Conduction-cooled XMC modules

To support the industry drive to open standards on conduction-cooled cards, the XMC site mechanical interfaces follow the VITA 20-2001 (R2005) conduction-cooled PCI Mezzanine Card (PMC) standard. To optimize the thermal transfer from XMC modules to the basecard the standard VPX3-1703 thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2005.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and the Curtiss-Wright TherMax™ thermal frame design provides optimum cooling for conduction-cooled XMC modules, allowing for higher power XMCs and/or increased long-term reliability through lower component temperatures.

## Timing resources

The VPX3-1703 provides a number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in the table below.

TABLE 2 VPX3-1703 timing resources

| TIMER | IMPLEMENTATION | TYPE | SIZE | TICK RATE/ PERIOD | MAXIMUM DURATION |
|---|---|---|---|---|---|
| LS1043A Flextimers | LS1043A | Free running counter with pre-settable initial & final values, programmable interrupt on counter event | 16-bit (8) 32-bit (4) | 3.125-200 MHz / 5-320 nsec | 1374 sec |
| RTC Alarm | RTC | Alarm interrupt | - | 1 Hz/ 1 sec | 200 years |
| Watchdog Timer | Monitor PLD | Presettable, Readable Downcounter with interrupt or reset on terminal count | 25-bit | 1 MHz/ 1 µsec | 33.6 sec |
| Safety Watchdog | LTC6993 Timer Blox | Factory configured rest time | - | 1 µsec | 3 sec |
| Elapsed Time Counter (ETC) | DS1682 Elapse Timer Counter | Factory programmed total elapsed time recorder | 32-bit | 0.25 sec | 34 years |

### XMC specifications

- PCIe interface: 4-lane PCIe Gen2 as per VITA 42.3
- Pn6 I/O: 20 different pairs and 24 single-ended to VITA 46.9 P2w1-X24s+X8d+X12d
- Routing: 100 Ohm differential, 50 Ohm single ended for Pn6 I/O signals
- 3.3V power: Provided from backplane 3.3V (Vs2)
- VPWR power: Drawn from backplane 5.0V (Vs3)
- +/-12 V_AUX, 3.3V: Routed to XMC site but not used by card
- Maximum supported XMC power: 20W

### Status indicators and controls

The VPX3-1703 SBC provides fail status by illuminating a red front panel LED in the event the diagnostics detect a card failure. The SBC also provides a user-controllable, green front panel status LED.

### COP emulator interfaces

The VPX3-1703 provides access to the processor COP interface for on-chip debugging. Consult the Hardware User's Manual for more information if you need to use a COP emulator with the VPX3-1703.

### Temperature sensors

The VPX3-1703 provides temperature sensors to measure board and processor temperatures. There are two sensors to measure temperature on the card and one sensor to directly measure the die temperature of the processor using its thermal diode feature. The sensors can be read by software and may be configured to generate an interrupt in case of an over temperature condition.

## LS1043A Trust Architecture and Secure Boot

The VPX3-1703 supports the Trust Architecture of the LS1043A for customers wanting to take advantage of these features. Please contact Curtiss-Wright for additional information.

## Software Support

### U-Boot firmware and monitor

The monitor provides a command line interface over serial port to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

Built-in-Test (BIT) - a library of diagnostic routines to support Power-up BIT (PBIT) and Initiated BIT (IBIT) are designed to provide 95% fault coverage.

### Operating system software

The VPX3-1703 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported for the VPX3-1703:

- 64-bit Linux BSP based on NXP SDK from Curtiss-Wright
  - The Linux BSP does not support the same level of BIT as does the VxWorks BSPs
- 64-bit VxWorks 7 64-bit SMP BSP

# Thermal Cooling

## TherMax-style thermal frame

Applicable to conduction-cooled cards, a TherMax thermal frame provides an unbroken metallic path from the XMC sites and shunted components to the back-side cooling surface of the card, thereby minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB, which has a high thermal resistance compared to aluminum.

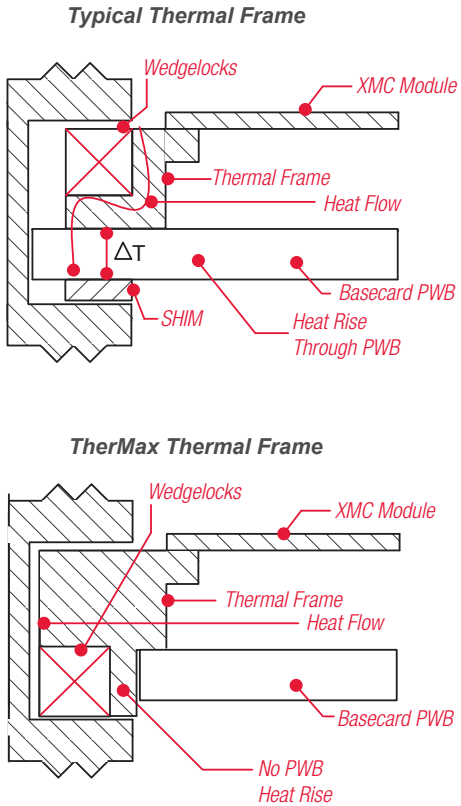


Figure 2: TherMax diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame

## Full-width thermal interface to back-side slot wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the VPX3-1703, the thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 3. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long term reliability. During test and integration activities where it may be desirable to install a conduction-cooled VPX3-1703 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

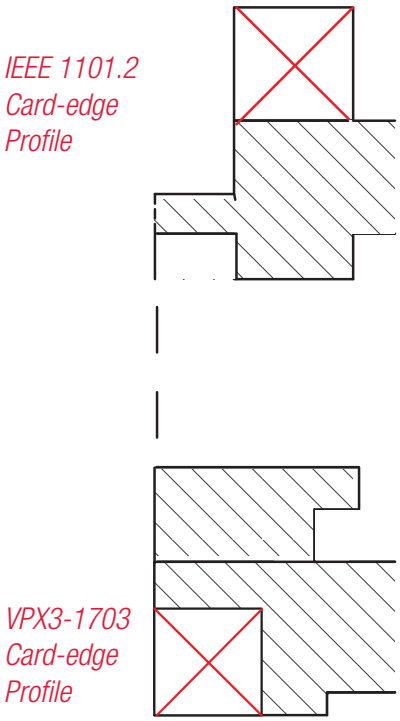


Figure 3: Card-edge profile deviates from IEEE 1101.2

VPX3-1703 card-edge profile is optimized to provide a full-width thermal interface to the back-side slot wall

# Rear Transition Module

To gain access to the backplane I/O signals of the VPX3-1703, the RTM3-131 rear transition module (RTM) is available to access I/O in a lab environment. There are several variants of the RTM to match the VPX3-1703 variants. Please contact the factory for more information.

# Specifications

## VPX3-1703 air-cooled cooling requirements

- Configuration: Power estimates are for VPX3-1703-A15A001
- Temperature range: -40 to 71°C
- Air-flow: 15 CFM

Note: Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The air-flow specifications are for worst case (highest power) conditions, with a 20W XMC installed. Curtiss-Wright can supply additional recommendations for specific power/temperature/altitude scenarios and pressure drop characteristics of the VPX3-1703 to support the design and testing of cooling subsystems. Please contact factory for assistance.

## Ruggedization levels

- Air-cooled cards are available in Levels 0, 100.
- Conduction-cooled cards are available in Levels 200, 300.

Please see the Curtiss-Wright Ruggedization Guidelines product sheet for more information.

TABLE 3 Dimensions and weight

| OPTION | DIMENSIONS | WEIGHT (grams) - Estimates |
|---|---|---|
| Air-cooled Level 0 | per VITA 46/IEEE 1101.1 | 300 |
| Air-cooled Level 100 | per VITA 46/IEEE 1101.1 | 300 |
| Conduction-cooled L200 | per VITA 46/IEEE 1101.2 | 375 |
| Conduction-cooled L300 LRM | per VITA 48.2 | 530 |
| RTM3-131 | per VITA 46 | 164 |

Notes:

1. The air-cooled format is designed to fit a chassis with 1.0” slot pitch, and shipped with 1” faceplates. A 0.8” variant can be available upon customer request.
2. Air-cooled cards available in temperature ranges L0 and L100.
3. Refer to the deviation from IEEE 1101.2 in Figure 3.
4. Refer to Ruggedization Guidelines product sheet for more information.

TABLE 4 Power requirements

| VOLTAGE | RUGGEDIZATION LEVEL | TYPICAL (TBC) | TYPICAL MAX (TBD) |
|---|---|---|---|
| 5V (Vs3) | L0 AC | 14W | 16W |
| | L100 AC | 16W | 18W |
| | L200 CC | 18W | 20W |
| 3.3V (Vs2) | Only routed to XMC | | |
| +3.3V_AUX | Only used to to pull up and buffer backplane system signals, and is routed to the IPMI, CPU RTC and XMC site | | |
| 12V (Vs1) | Only routed to XMC | | |
| +/-12V_AUX | Only routed to XMC | | |

Notes:

1. Power estimates are for VPX3-1703-xxxA001. No mezzanine installed.
2. All power rails defined as in VITA 46.0 for 3U basecards.

TABLE 5 OpenVPX slot/module profile support

| SLOT PROFILE | MODULE PROFILE | 1703 VARIANT |
|---|---|---|
| SLT3-PAY-2F2U-14.2.3 | MOD3-PAY-2F2U-16.2.3-2 | VPX3-1703-xxxx1xx |
| SLT3-PAY-2F2U-14.2.3 | MOD3-PAY-2F2U-16.2.3-3 | VPX3-1703-xxxx1xx |
| SLT3-PAY-1F1F2U-14.2.4 | MOD3-PAY-1F1F2U-16.2.4-3 | VPX3-1703-xxxx1xx |
| SLT3-PAY-1F1F2U-14.2.4 | MOD3-PAY-1F1F2U-16.2.4-4 | VPX3-1703-xxxx1xx |
| SLT3-PAY-2F2T-14.2.5 | MOD3-PAY-2F2T-16.2.5-2 | VPX3-1703-xxxx0xx |
| SLT3-PAY-2F2T-14.2.5 | MOD3-PAY-2F2T-16.2.5-3 | VPX3-1703-xxxx0xx |
| SLT3-PAY-2F-14.2.7 | MOD3-PAY-2F-16.2.7-1 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |
| SLT3-PAY-2F-14.2.7 | MOD3-PAY-2F-16.2.7-2 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |
| SLT3-PAY-1F2U-14.2.12 | MOD3-PAY-1F2U-16.2.11-1 | VPX3-1703-xxxx1xx |
| SLT3-PAY-1F2U-14.2.12 | MOD3-PAY-1F2U-16.2.11-2 | VPX3-1703-xxxx1xx |
| SLT3-PER-2F-14.3.1 | MOD3-PER-2F-16.3.1-2 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |
| SLT3-PER-2F-14.3.1 | MOD3-PER-2F-16.3.1-3 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |
| SLT3-PER-1F-14.3.2 | MOD3-PER-1F-16.3.2-1 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |
| SLT3-PER-1F-14.3.2 | MOD3-PER-1F-16.3.2-2 | Either VPX3-1703-xxxx0xx or VPX3-1703-xxxx1xx |

# Ordering Information

The VPX3-1703 is ordered with the following part numbers. VPX3-1703-UVWXYPZ, where U, V, W, X, Y, P and Z denote cooling method, temperature range, mechanical format and functional configuration respectively. Not all possible configurations are offered, consult Curtiss-Wright for available configurations.

TABLE 6 Ordering information - VPX3-1703-uvwxypz

| PART NUMBER | AVAILABLE OPTIONS |
|---|---|
| Form Factor | 3U VPX (VITA 46 and 48) |
| Model number | 1703 |
| u: Cooling Method | A: Air cooled<br>C: Conduction cooled |
| u: Ruggedization Level | 0: Level 0 (0 to 50ºC)<br>1: Level 100 (-40 to 71ºC)<br>2: Level 200 (-40 to 85ºC)<br>9: Customized |
| w: Mechanical Format | 1: 0.80” pitch, 2-level maintenance covers included<br>3: 0.85” pitch, 2-level maintenance covers included<br>5: 1” pitch, no 2-level maintenance covers<br>9: Customized<br>Others: Reserved |
| x: Data Plane Mode | A: Two x4 Gen 2 ports (software configurable)<br>Four x2 Gen 2 ports (software configurable)<br>Eight x1 Gen 2 ports with 2 NTB (software configurable)<br>B: Eight x1 Gen 2 ports with 6 NTB (factory configurable)<br>Others: Reserved |
| y: Ethernet/Control Plane Mode | 0: 2 x 1000BASE-T<br>1: 2 x 1000BASE-X<br>9: Customer specific<br>Others: Reserved |
| p: Process/Memory Config | 0: 1.6Ghz, 4 GB DDR4, 4 GB eMMC<br>2: 1.0Ghz, 4 GB DDR4, 4 GB eMMC<br>4: 1.6Ghz, 4 GB DDR4, 64 GB eMMC<br>6: 1.0Ghz, 4 GB DDR4, 64 GB eMMC<br>Others: Reserved<br>Notes:<br>1. Default eMMC size on standard product is 4 GB SLC.<br>2. Default for larger size eMMC is 64 GB.<br>3. Other configurations will be treated as customer-specific variants. |
| z: I/O Mode | 0: XMC with X24s+X8d+X12d, one SATA2, two EIA232, two EIA422, two DIO-in, two DIO out, two USB, with IPMC<br>1: XMC with X24s+X8d+X12d, one SATA2, two EIA232, two EIA422, four DIO-in, three DIO out, card_fail<br>Others: Reserved |

Notes:

1. Not all combinations of an orderable variant are available as standard product. Variants highlighted in yellow are standard product.
2. Please consult your local sales office for further help in selecting the appropriate variant.
3. Air cooled variants are delivered with a 1” faceplate. 0.8” variants are available, please consult factory.
4. Backplane configuration is default to what is specified. This can be reconfigured by customer.
5. LRM covers are only available for conduction-cooled cards.

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