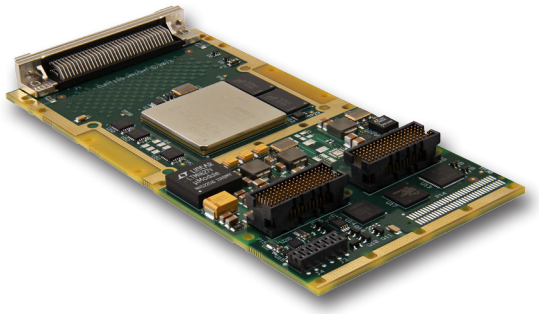
XF07-523

Xilinx Kintex-7 based XMC with LVDS I/O Ports

CURTISSWRIGHTDS.COM



Key Features

- Xilinx user programmable Kintex-7 325T FPGA
- 2 x banks of 16-bit x 128M DDR3 SDRAM (total 512 Mbytes)
- XMC format
- VxWorks and Linux host support
- Air- and conduction-cooled variants

Applications

- Radar
- SIGINT/ELINT
- EW

Overview

The XF07-523 is a high performance user-programmable FPGA resource coupled to fast LVDS data I/O ports in an XMC format module.

The XF07-523 is a member of the XF07 family of products, all based on the Xilinx® 7-Series FPGA. Functionally, the family includes fiber-optic and analog I/O variants based on a common processing building block.

The combination of direct high-speed I/O ports and next generation FPGA processing makes the XF07-523 ideal for demanding applications including radar, imaging and test equipment across commercial and defense market spaces.

Xilinx Kintex-7 FPGA

The XF07-523 is built around a user programmable Xilinx Kintex-7 325T FPGA resource (speed grade 2). Kintex-7 is a member of Xilinx's 28nm 7-Series family which also includes Artix-7 and Virtex®-7 members. The FPGA is supported by high speed DDR3 memory resources directly connected the FPGA.

The FPGA configuration images can be stored in the Flash memory which can be updated and controlled by the host CPU using the PCI Express® (PCIe) interface. The FPGA can be reconfigured from images indexed in the Flash including a write protected recovery configuration. FPGA configuration from Flash can also take advantage of AES encryption.

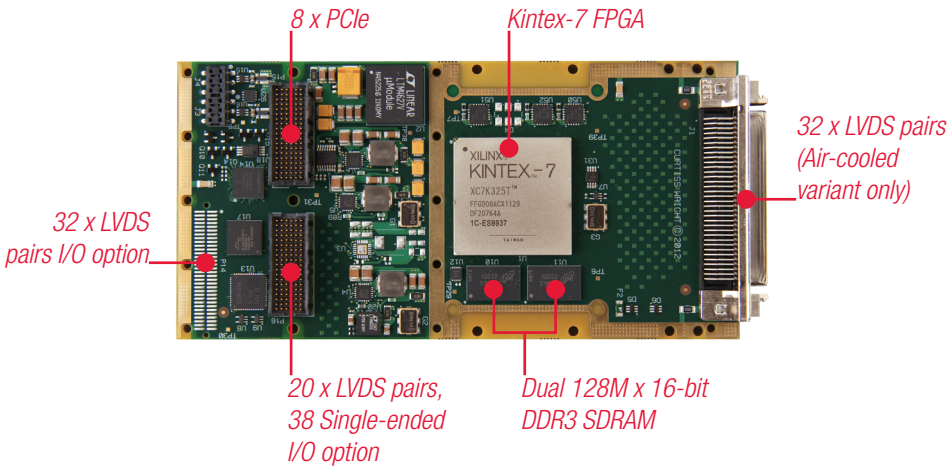


Figure 1: XF07-523 key features

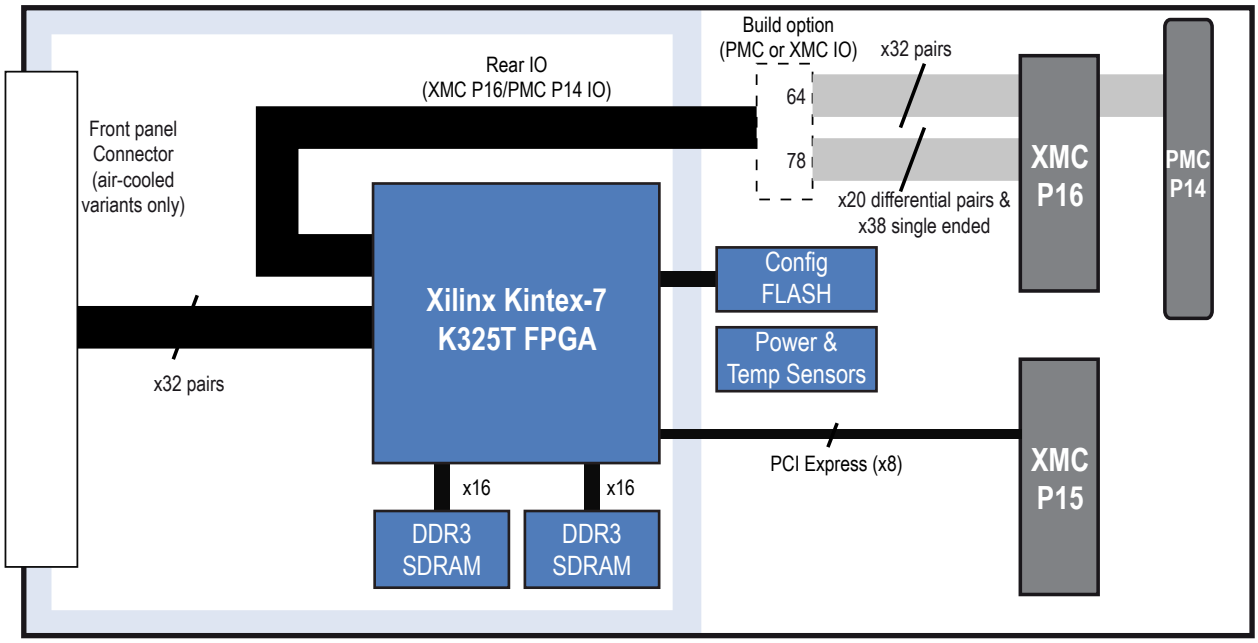


Figure 2: XF07-523 block diagram

Specifications

FPGA

- Device: Xilinx Kintex-7 K325T (speed grade 2)
- Configuration
  - 1 Gbit Flash (FPGA boot/configuration including recovery image)
  - JTAG/ChipScope™ Pro port

Front panel I/O - air-cooled only builds

- Number of LVDS: 32 x differential pairs
- Connector type: SCSI-II type connector

Rear I/O (build option)

- Number of LVDS: 32-differential pairs
  - 20 x differential pairs + 38 x single-ended (XMC)
  - 32 x differential pairs (PMC)
- Connector: XMC P16 or PMC P14 (build options)

Memory

- Type: DDR3 SDRAM
- Capacity:
  - Total: 512 MB
  - Arranged as two banks, each 128M x 16-bit
- Bandwidth: 2.5 Gbytes/sec

XMC interface

- Compliance: VITA 42.0
- XMC P15:
  - 8 x RocketIO GTP or
  - 4 x / 8 x PCIe release 2

Software/HDL

- Host Drivers: VxWorks®, Linux® Fedora™
- Support/Utilities:
  - FusionXF™ Development Kit
  - FPGA/Flash programming, diagnostics
- HDL examples: Memory interfaces, PCIe, data DMA

Miscellaneous

- Weight:
  - Air-cooled variants: 148g
  - Conduction-cooled variants: 132g
- Power: 17.5 typ (FPGA load dependant)

TABLE 1 Environmental specifications

QUALIFICATION		AIR-COOLED			CONDUCTION-COOLED	
		LEVEL 0	LEVEL 100	LEVEL 200 (Note 6)	LEVEL 100	LEVEL 200
Temperature	Operational, (AC, see Note 4) (CC, see Note 7)	0 to +50°C	-40 to +71°C	-40 to +85°C	-40 to +71°C	-40 to +85°C
	Non-operational (storage)	-40 to +85°C	-55 to +125°C	-55 to +125°C	-55 to +125°C	-55 to +125°C
Vibration	Sine (see Note 1)	2g peak 15 to 2k Hz	10g peak 15 to 2k Hz	10g peak 15 to 2k Hz	10g peak 15 to 2k Hz	10g peak 15 to 2k Hz
	Random (see Note 2)	0.01 g^2/Hz 15 to 2k Hz	0.04 g^2/Hz 15 to 2k Hz	0.04 g^2/Hz 15 to 2k Hz	0.1 g^2/Hz 15 to 2k Hz	0.1 g^2/Hz 15 to 2k Hz
Shock, operational (Note 3)		20g peak	30g peak	30g peak	40g peak	40g peak
Humidity	Operational	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing
	Non-operational (storage)	0 to 95% non-condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing
Conformal coating (Note 5)		No	Yes	Yes	Yes	Yes

Notes:

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type is manufacturing site specific. Consult the factory for details.
6. This is a non-standard product. Consult factory for availability.
7. Temperature is measured at the card edge.

Multiple Memory Banks

The XF07-523 supports two banks of 128M x 16-bit DDR3 SDRAM, each directly connected to the FPGA. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. Each memory bank supports read or write bandwidths of up to 2.5 Gbytes/sec.

PCIe & Multi-GB/s I/O

The XF07-523 supports a x8/x4 PCIe channel through the primary XMC P15 connector using the FPGA's built-in PCIe end-point block. Alternatively, the XMC P15 can be used to provide user defined protocol support over the data links, such as Aurora™ for higher bandwidth and lower latency operation. However, this mode would require customer HDL development for new modes.

Front Panel Digital I/O

For air-cooled build variants, 32 differential [LVDS] pairs are provided through a SCSI-II type front panel connector. These signals are directly connected to the XF07-523's FPGA.

PMC P14 and XMC P16 Digital I/O

In addition to front panel I/O, the XF07-523 can provide up to 64 digital I/O signals, routed as differential pairs to the PMC P14 connector. Alternatively, 78 signals are routed to the XMC P16 connector support with a mix of differential and single-ended signals. These I/Os are directly connected to the FPGA. PMC or XMC based I/O are mutually exclusive build options and available for all environmental build options.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities complete with examples for using the XF07-523. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively. FusionXF allows user applications to be associated standard drivers, thereby speeding up application development.

Software utilities are provided for configuring the FPGA. These include Flash programming and configuring the FPGA from one of many indexed images in Flash.

FusionXF supports VxWorks and Linux Fedora operating systems. Additional operating systems, such as Windows®, or other distributions can be considered on request.

Rugged Build Options

A range of environmental requirements are addressed by the XF07-523 including commercial, air-cooled rugged and conduction-cooled.

Ordering Information

TABLE 3 Ordering information

PART NUMBER	DESCRIPTION	FRONT PANEL I/O	PMC P14 I/O	XMC P16 I/O	RUGGEDIZATION LEVEL
XF07-523-A001040	XC7K325T (-2I) XMC (PCIe x8)	32 LVDS pairs	32 LVDS pairs	-	Air-cooled, Level 0
XF07-523-A001060	XC7K325T (-2I) XMC (PCIe x8)	32 LVDS pairs	-	20 LVDS, 38 SE	Air-cooled, Level 0
XF07-523-A101040	XC7K325T (-2I) XMC (PCIe x8)	32 LVDS pairs	32 LVDS pairs	-	Air-cooled, Level 0
XF07-523-A101060	XC7K325T (-2I) XMC (PCIe x8)	32 LVDS pairs	-	20 LVDS, 38 SE	Air-cooled, Level 0
XF07-523-C200040	XC7K325T (-2I) XMC (PCIe x8)	-	32 LVDS pairs	-	Conduction-cooled Level 200
XF07-523-C200060	XC7K325T (-2I) XMC (PCIe x8)	-	-	20 LVDS, 38 SE	Conduction-cooled Level 200
XF07-523-XFL	Linux FusionXF SDK/ HDK for XF07-523	N/A	N/A	N/A	N/A
XF07-523-XFV	VxWorks FusionXF SDK/ HDK for XF07-523	N/A	N/A	N/A	N/A