XF07-RLDRAM

Xilinx® Kintex-7 Based Co-Processor XMC with HSS I/O

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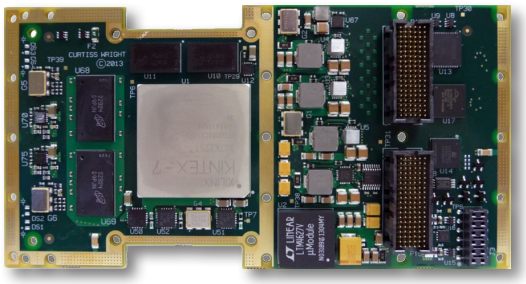

Key Features

- Xilinx® user-programmable Kintex™-7 325T or 410T FPGA
- 2 x banks of 16-bit x 128M DDR3 SDRAM (total 512 Mbytes)
- 2 x banks of 16M x 36-bit RLDRAM
- x8 High Speed Serial (HSS) links to XMC P16 for Aurora, sFPDP, Ethernet, etc.
- XMC format
- VxWorks® and Linux® host support
- Air- and conduction-cooled variants

Applications

- Radar
- SIGINT/ELINT
- EW
- Camera interfaces (e.g. Camera Link®)

Overview

The XF07-RLDRAM is a high-performance user-programmable FPGA resource supporting both fast DDR3 SDRAM and RLDRAM memory banks for FPGA based co-processing applications.

The combination of direct high-speed I/O ports and next generation FPGA processing makes the XF07-RLDRAM ideal for demanding applications, including radar, imaging, and test equipment across commercial and defense market spaces.

The XF07-RLDRAM is a member of the XF07 family of products, all based on Xilinx's 7-Series FPGA. Functionally, the family includes LVDS digital and analog I/O variants based on a common processing building block.

Xilinx Kintex™-7 FPGA

The XF07-RLDRAM is built around a user-programmable Xilinx Kintex-7 FPGA resource (speed grade 2).The FPGA configuration images can be stored in the Flash memory which can be updated and controlled by the host CPU using the PCI Express® (PCIe) interface. The FPGA can be reconfigured from images indexed in the Flash including a write protected recovery configuration. FPGA configuration from Flash can also take advantage of AES encryption.

Multiple Memory Banks

The XF07-RLDRAM supports two banks of 128M x 16-bit DDR3 SDRAM, each directly connected to the FPGA. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. Each memory bank supports read or write bandwidths of up to 2.5 Gbytes/sec.

Dual banks of RLDRAM, with each banks 16M x 36-bit, provides low latency memory access. Each RLDRAM memory bank supports bandwidths of up to 4.5 Gbytes/sec.

PCI Express I/O

The XF07-RLDRAM supports a x8/x4 PCIe channel through the primary XMC P15 connector using the FPGA's built-in PCIe endpoint block.

High Speed Serial Link I/O

In addition to the PCIe port, eight full duplex HSS links are routed to the XMC P16 connector. The HSS links are fully user programmable and are directly linked to the Kintex-7 FPGA.

Customers can program the FPGA with protocols as required for the end application (e.g., Aurora, sFPDP, Ethernet, and others). See Table 1 for pinout.

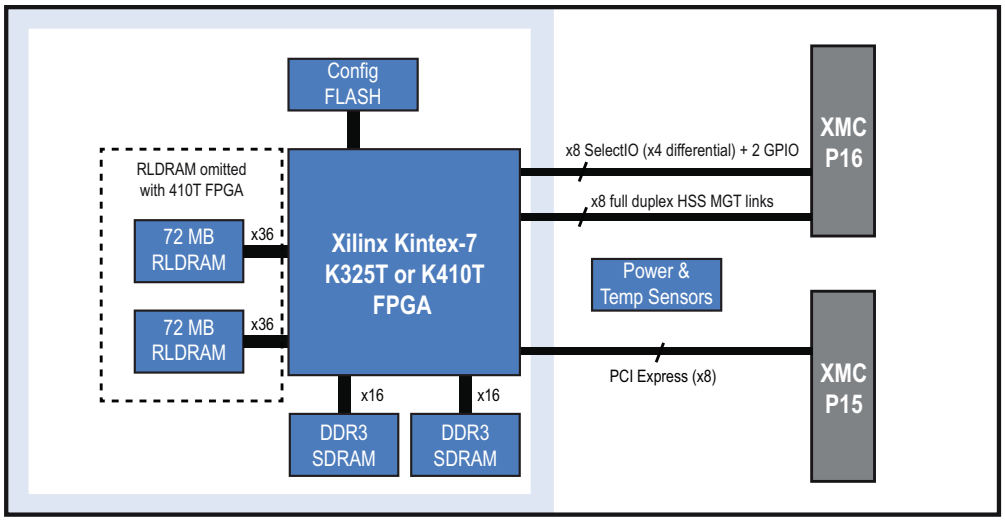

Figure 1: XF07-RLDRAM block diagram

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities complete with examples for using the XF07-523. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively. FusionXF allows user applications to be associated with standard drivers, thereby speeding up application development.

Software utilities are provided for configuring the FPGA. These include Flash programming and configuring the FPGA from one of many indexed images in Flash.

FusionXF supports Wind River® VxWorks and Linux operating systems. Fedora, CentOS and Red Hat Enterprise Linux are supported, and other Linux distributions can be considered on request.

Specifications

FPGA

- Xilinx Kintex-7 K325T (speed grade 2) OR Xilinx Kintex-7 K410T (speed grade 2, no RLDRAM fitted with this FPGA type)
- Configuration:
  - 1Gbit Flash (FPGA boot/configuration including recovery image), programmed over PCIe interface
  - JTAG/ChipScope Pro port

Memory

- DDR3 SDRAM capacity
  - Total: 512 MB
  - Two banks, each 128M x 16-bit
- DDR3 SDRAM speed: 2.5 Gbytes/sec
- RLDRAM capacity (not fitted with 410T FPGA variant)
  - Total: 144 Mbytes
  - Two banks, each 16M x 36-bit
- RLDRAM speed: 4.5 Gbytes/sec

XMC Interface

- Compliance: VITA 42.0
- XMC P15:
  - 8x RocketIO GTP or
  - x4/x8 PCIe release 1.1
- XMC P16
  - 8x full duplex links connected to FPGA
  - 2x differential SelectIO (or 4x single-ended SelectIO)
  - 2 x single-ended I/O

Software/HDL

- Host Drivers: VxWorks, Linux
- Support/Utilities: FusionXF development kit FPGA/Flash programming, diagnostics
- HDL examples: Memory interfaces, PCIe, data DMA

Miscellaneous

- Weight: 166g
- Power: 30W
- MTBF: Contact factory

TABLE 1 Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	RIO_TX_P_8	RIO_TX_N_8	USER_SE0	RIO_TX_P_9	RIO_TX_N_9	NC
2	GND	GND	USER_SE1	GND	GND	NC
3	RIO_TX_P_10	RIO_TX_N_10	NC	RIO_TX_P_11	RIO_TX_N_11	NC
4	GND	GND	NC	GND	GND	NC
5	RIO_TX_P_12	RIO_TX_N_12	NC	RIO_TX_P_13	RIO_TX_N_13	NC
6	GND	GND	NC	GND	GND	NC
7	RIO_TX_P_14	RIO_TX_N_14	NC	RIO_TX_P_15	RIO_TX_N_15	NC
8	GND	GND	NC	GND	GND	NC
9	USER_LVDS_P_0	USER_LVDS_N_0	NC	USER_LVDS_P_1	USER_LVDS_N_1	NC
10	GND	GND	NC	GND	GND	NC
11	RIO_RX_P_8	RIO_RX_N_8	NC	RIO_RX_P_9	RIO_RX_N_9	NC
12	GND	GND	NC	GND	GND	NC
13	IO_RX_P_10	RIO_RX_N_10	NC	RIO_RX_P_11	RIO_RX_N_11	NC
14	GND	GND	NC	GND	GND	NC
15	RIO_RX_P_12	RIO_RX_N_12	NC	RIO_RX_P_13	RIO_RX_N_13	NC
16	GND	GND	NC	GND	GND	NC
17	RIO_RX_P_14	RIO_RX_N_14	NC	RIO_RX_P_15	RIO_RX_N_15	NC
18	GND	GND	NC	GND	GND	NC
19	USER_LVDS_P_2	USER_LVDS_N_2	NC	USER_LVDS_P_3	USER_LVDS_N_3	NC

Environmental Specification

- Temperature
  - Operational: -40°C to +85°C
  - Storage: -55°C to +125°C
  - Temperature is measured at the card edge.
- Vibration
  - Sine: 10g peak, 15-2k Hz
    - Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15-44 Hz, depending on specific test equipment.
  - Random: 0.1g^2/Hz, 15-2k Hz
    - Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
- Shock: 40g peak
  - Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
- Humidity
  - Operational: 0-100% non-condensing
  - Storage: 0-100% condensing
- Conformal Coat: Yes
  - Conformal coating type is manufacturing site specific. Consult the factory for details.

Ordering Information

TABLE 2 Ordering Information

PART NUMBER	DESCRIPTION
XF07-523-C200062LF	Customer-specific version of XF07-523-C200064LF
XF07-523-C200064LF	Conduction-cooled, K325T-2 FPGA, RLDRAM, P16 HSS I/O
XF07-523-C210065LF	Conduction-cooled, K410T-2 FPGA, no RLDRAM, P16 HSS I/O