DBS-120PC

PCMCIA Card - 20 Mbps PCM Bit Sync/Decom

CURTISSWRIGHTDS.COM

Key Features

- PCMCIA-based bit synchronizer/ data decommutator
- Low power 3.3 VDC operation
- Windows compatible driver software included
- Supported by third party data analysis software
- Bit sync:
  - + Bit rates up to 20 Mbps, NRZ codes
  - + Input signal amplitudes from 0.1 to 5.0 volts p-p
  - + Accepts all IRIG 106 PCM inputs
  - + Provides all IRIG 106 PCM data outputs with coherent clock
  - + On-board bit error rate detector and test data simulator
  - + Includes clock sync indication
- Decom:
  - + PCM input rate up to 20 Mbps
  - + Accepts RS-422, or TTL input data and clock
  - + Onboard minor frame timestamp
  - + RS-422 and TTL outputs

Applications

- Portable preflight test
- Data analysis
- Data archival
- Flight test instrumentation

Overview

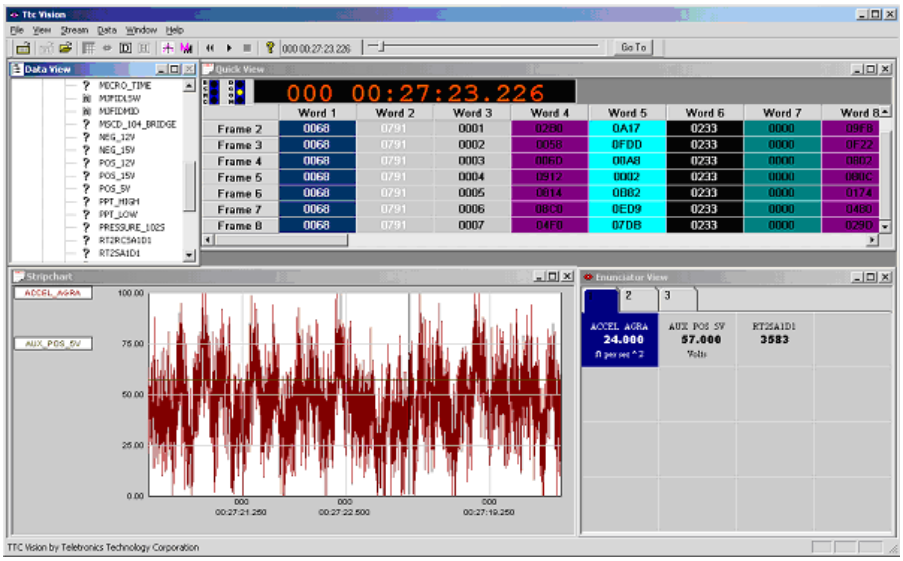
The DBS-120PC combines the functions of bit synchronization and data decommutation into a single low cost PCMCIA type II card. The card can be installed in a portable PC compatible platform for preflight or lab test. The bit synchronizer provides full featured clock reconstruction, data recovery and code conversion. The bit sync accepts PCM inputs at rate of up to 20 Mbps for NRZ codes and up to 10 Mbps for BiØ codes with amplitudes from 0.1 to 5.0 Volts p-p. The bit sync input impedence is programmable to 50Ω, 75Ω or 10kΩ. TTL and RS-422 compatible PCM data and 0°/180° clock bit sync outputs are provided. The bit sync output is also internally connected to the on-card decom. A Bit Error Rate (BER) measurement capability with an on-card test data simulator is included to allow characterization of data link quality. The data decommutator provides full IRIG frame synchronization and data decommutation. The decom accepts PCM data at rates up to 20 Mbps from the on-card bit sync or an external source. The decom external data and clock input is programmable for RS-422, 10KΩ TTL, or 75Ω TTL. Decommutated data words and frame timestamp are made available via the PCMCIA bus for analysis, archival, and monitoring.

Additional Features

- Compatible with Curtiss-Wright's
  - + USB-100 board and USB-100 module
  - + DCOM-112 PCMCIA decom
  - + BSM series PCMCIA bit sync cards
  - + DBS-120PC PCMCIA/CardBus Decom and BitSync
  - + TTCWare programming and setup software application
- Displays PCM data in real time or from archived files
- All named parameters are accessible from a tree-based view
- Allows PCM parameter concatenation
- Will create and play back data archives
- Seek to any location in an archive either by position or by entering the desired time
- Will convert from PCM counts to engineering units using eighth order polynomials
- Quick look display shows raw data in either decimal or hexadecimal
- Up to sixteen variables can be plotted on a strip chart
- Data can be output from a selection on the strip chart into Excel
- Enunciator display shows EU values and indicates range-based alarms
- Four H.261 video channels can be displayed
- Supports CVSD audio
- Uses either PCM header time or configurable embedded time (binary and BCD)

TTC Vision™

Quickly analyze real-time and/or archived PCM data and graphically display the results all from within an intuitive Windows environment. This unique software tool supports integration, validation and maintenance of Curtiss-Wright's data acquisition systems and is the perfect quick-look data support tool for use within the flight test environment.



Data Concatenation

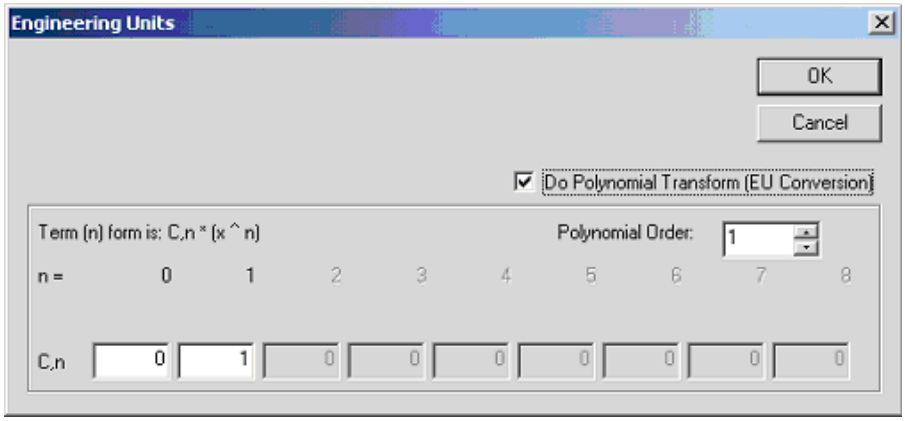
Concatenated values can be produced by sequencing bit ranges from within raw PCM data values. Up to four parameters may be combined to produce a single concatenated value. Beneath each parameter name in the Edit Concatenation dialog box is a control containing a hexadecimal value that corresponds to a mask (or bit field) identifying which bits in the parameter will be used to calculate the concat. This value can be changed using the arrow buttons on either side of the control.

Engineering Units Conversion

Conversion from raw PCM counts to more meaningful values is done using the following polynomial formula:

$y = Cn \times n + Cn\text{-}1xn\text{-}1 + \ldots + C0$

where n is the order of the polynomial and x is the value in raw counts. The order of the polynomial and constant C for each term can be set (for up to 9 terms) using the Engineering Units dialog box.



Specifications

General

- PCMCIA bus: Interface for setup/control/status/power
- Supply current: +3.3V @ 600mA
- Operating temperature: 0° to +50°C (box ambient temp)
- Storage temperature: -20° to +85°C

Dimensions and Mechanical

- Compatibility: PCMCIA type II cardbus
- Weight: 4 oz. (105 grams)
- Unit connectors (2): PCMCIA 15P plug

BIT SYNCHRONIZER

Input Data

- PCM inputs: Single-ended analog or differential RS-422, programmable
- Input codes: NRZ-L/M/S, RNRZ-L (fwd/rev) or BiØ-L/M/S per IRIG STD 106-01, programmable
- Analog input level: 0.1 to 5 volts p-p
- Analog DC offset: Up to ±10 volts
- Analog input impedance: 50Ω, 75Ω or 10 KΩ, programmable
- Bit rate: NRZ Codes - Programmable from 80 Kbps to 20 Mbps. BiØ Codes -
- Programmable from 40 Kbps to 10 Mbps

Performance

- Loop bandwidth: 0.01% to 1.0% of bit rate, programmable
- Bit error probability: Within 2.5 dB of theoretical BER curve to Eb/No = 3dB
- BER measurement: Measures errors on a 15 bit pseudo random pattern. Up to 255 error counted over (up to) 255M clock periods per measurement.

Outputs

- PCMCIA bus: Interface for setup/control/status/power
- PCM data: Programmable PCM data output, TTL and RS-422 compatible
- Output codes: NRZ-L/M/S, RNRZ-L (fwd/rev), BiØ - L/M/S per IRIG 106-01, programmable
- Output clock: 0° or 180°, programmable TTL and RS-422 compatible
- Clock sync. indicator: TTL compatible

Simulator

- Simulator data: 15 bit pseudo random pattern or programmable frame pattern, programmable, TTL compatible
- Simulator codes: NRZ-L/M/S, RNRZ-L (fwd/rev) or BiØ-L/M/S per IRIG 106-01, programmable
- Simulator clock: 0°, TTL compatible

DECOMMUTATOR

Input Data

- Inputs: NRZ-L data and clock
- Polarity: Programmable for normal (0°), or inverted (180°)
- Impedance: RS-422, TTL 75Ω, TTL 10 KΩ, programmable for clock and data
- Rate: Up to 20 Mbps
- Time source: Internal counter or seeded time from the PC

Processing

- Sync pattern: Up to 32 bits programmable
- Sync mask: Any bit/s mask, programmable
- Lock strategy: Programmable for 1 to 16 good frames to acquire LOCK
- Drop lock: Programmable for 1 to 16 bad frames to drop LOCK
- Bit slip: 0, +/-1, +/-2, +/-3 bits programmable
- Bits per word: 8 to 16 programmable
- Time: Microsecond of the year for each minor frame
- Minor frame length: Up to 1024 words per minor frame
- Major frame length: Up to 256 minor frames per major frame
- Major frame: Sub-frame commutation is handled by PC application
- Major frame sync: SFID and sync bits
- SFID: Programmable at any word

Status Indicators (over Bus)

- Bit slip indicator bit
- Flywheel indicator bit
- Decom in check state
- Decom in search state
- Clock present indicator
- Data present indicator
- Minor frame lock indicator
- Major frame lock (by software application)

Ordering Information

Please contact Curtiss-Wright Defense Solutions.