DBS-140U

USB 2.0 - 40 Mbps PCM Bit Sync/Decom/Simulator

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Key Features

- USB 2.0 peripheral with bit synchronizer, data decommutator, and simulator
- IRIG-B time code reader and generator
- Windows compatible driver software included
- Supported by third party data analysis software

Applications

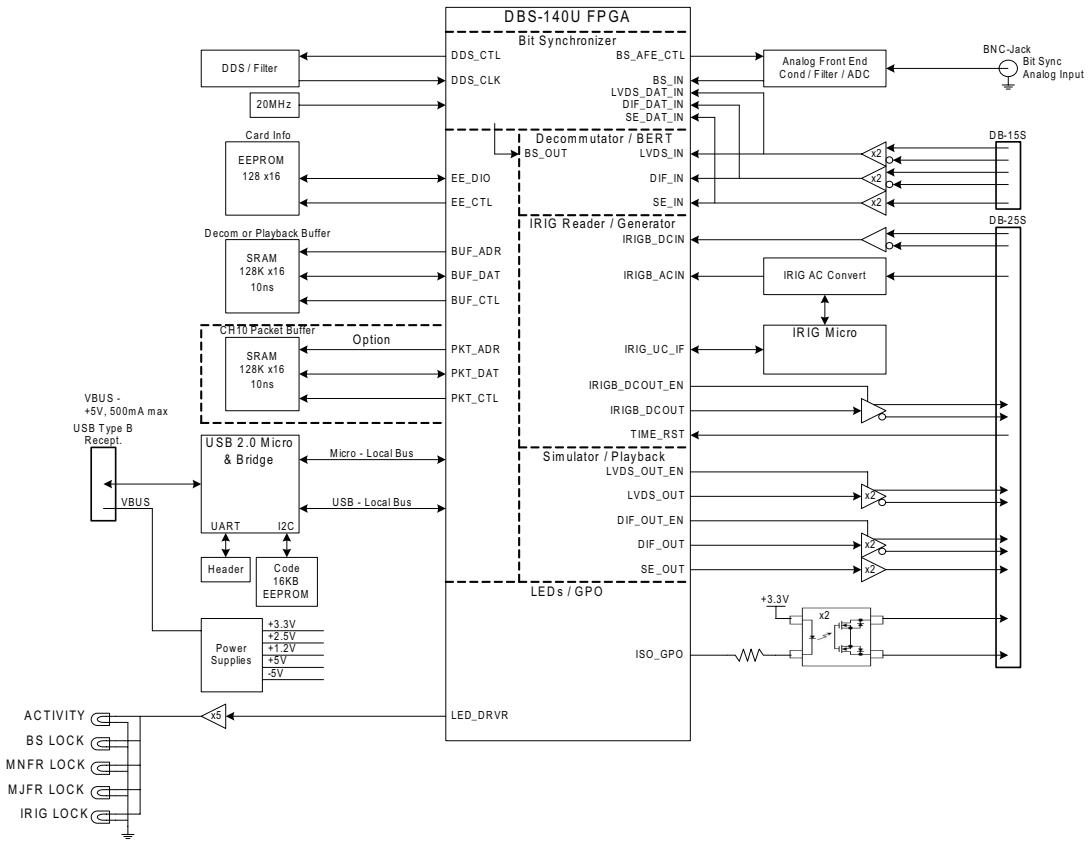
- Portable preflight test
- Data analysis
- Data archival
- Flight test instrumentation

Overview

The DBS-140U combines the functions of a bit synchronizer, data decommutator and simulator into a USB 2.0 peripheral. Bit synchronizer functionality provides full-featured clock reconstruction, data recovery and code conversion. Recovered PCM data and clock are routed to a data decommutator, bit error rate tester and output multiplexer. The data decommutator provides full IRIG frame synchronization and data decommutation at rates up to 40 Mbps. PCM processed by the decom is selected by the user. Data and clock sources include the bit synchronizer output and external differential/single-ended receivers. Decommutated data words and time tags (elapsed, Host time or IRIG-B) are made available to the computer via the USB port for analysis, archival, and monitoring. The bit error rate tester provides closed loop link testing by measuring the errors in the bit synchronizer data output. A simulator function allows playback of archived data from the computer via the USB port, transmission of programmable PCM format data or generation of pseudo-random patterns. Simulator data and clock are routed to the output multiplexer. Selected output, bit synchronizer or simulator is buffered by differential and single-ended drivers.

Additional Features

- Bit synchronizer
  - + TTL, RS422 , LVDS or analog selectable data inputs
  - + NRZ-L/M/S or RNRZ-L input codes at rates 0.030 to 30 Mbps; BiØ-L/M/S input codes at rates 0.030 to 15 Mbps
- Data decommutator/BERT
  - + Enhanced IRIG-106 Chapter 4 and Chapter 8 compatible
  - + Input rate up to 40 Mbps
  - + TTL, RS-422 or LVDS selectable external data and clock inputs
  - + Bit synchronizer internal input data and clock
  - + Onboard frame time tag - IRIG B, host time or elapsed
  - + PseudoRandom pattern receiver with error measurement: 7, 9, 11, 15, 20 or 23 type patterns
- Playback/simulator
  - + Regenerate archived PCM data at programmable rates of up to 40 Mbps
  - + Generate a programmable PCM format
  - + PseudoRandom pattern generator: 7, 9, 11, 15, 20 or 23 type patterns
  - + Provides all IRIG-106 PCM data outputs with coherent clock



DBS-140U Block Diagram

Specifications

General

- Operating configuration: The DBS-140U unit can be connected to any Windows XP or 7 compatible host computer with USB 2.0 ports
- Processor: 8051 type with a serial interface engine to handle USB transfers
- I/O: Provides interfaces for the following: USB 2.0 serial port, decom inputs (LVDS, RS-422 or SE), playback outputs (LVDS, RS-422 or SE), IRIG-B AC and DC inputs, isolated general purpose outputs

Serial Inputs

- Types: TTL single-ended, RS-422 differential, low voltage differential signaling (LVDS), analog
- Data rate:
  - TTL - minimum 30 Kbps; maximum 5 Mbps for NRZ codes or 2.5 Mbps for BiØ codes
  - RS-422 - minimum 30 Kbps; maximum 20 Mbps for NRZ codes or 10 Mbps for BiØ codes
  - LVDS - minimum 30 Kbps; maximum 40 Mbps for NRZ codes or 15 Mbps for BiØ codes
  - Analog - minimum 30 Kbps; maximum 30 Mbps for NRZ codes or 15 Mbps for BiØ codes.
  - Note: Data inputs to the bit synchronizer are limited to the maximums of 30 Mbps for NRZ codes and 15 Mbps for BiØ codes
- Signal characteristics:
  - TTL - Terminated by 10 KOhm to ground. Buffered by NC7WZ14PX (or equivalent). Normal or inverted data. 0 or 180 degree clock.
  - RS-422 - Terminated by 120 Ohm. Buffered by RS-422 compatible receiver with open, shorted or terminated input failsafe. Normal or Inverted data. 0 or 180 degree clock.
  - LVDS - Terminated by 100 Ohm. Buffered by EIA-644 compatible receiver with open, shorted or terminated input failsafe. Normal or Inverted data. 0 or 180 degree clock.
  - Analog:
    - Impedance - 50 Ohm, 75 Ohm or > 1 KOhm.
    - Level - 0.1 to 20 Vpp.
    - Offset - ±10 VDC.
    - Amplitude - ±10V combined level and offset

Serial Outputs

- Types: TTL single-ended, RS-422 differential, low voltage differential signaling (LVDS)
- Data rate:
  - TTL - minimum 30 Kbps; maximum 5 Mbps for NRZ codes or 2.5 Mbps for BØ codes.
  - RS-422 - minimum 30 Kbps; maximum 20 Mbps for NRZ codes or 10 Mbps for BiØ codes.
  - LVDS - minimum 30 Kbps; maximum 40 Mbps for NRZ codes or 15 Mbps for BiØ codes
- Signal characteristics:
  - TTL - Driven by NC7WZ14PX (or equivalent). Normal or inverted data. 0 or 180 degree clock. Enable or Disable (outputs driven to logic “0”). Cable length less than 3ft.
  - RS-422 - Driven by a RS-422 compatible driver. Normal or inverted data. 0 or 180 degree clock. Enable or Disable (outputs Tri-state).
  - LVDS - Driven by an EIA-644 compatible driver. Normal or inverted data. 0 or 180 degree clock. Enable or Disable (outputs Tri-state)
- Source: Simulator or bit sync (Note: each source can feed multiple output types)

USB Port

- Type: USB 2.0
- Signaling bit rates: High Speed (480 Mbps)
- Transfer rate: 5 Mbytes per second (8 bpw @ 40 Mbps)
- Direction: Uni-directional, transmit or receive

Bit Synchronizer

- Serial input: TTL single-ended, RS-422 differential, low voltage differential signaling (LVDS), analog
- Input codes: NRZ-L/M/S, BiØ -L/M/S or RNRZ-L. (Note: RNRZ-L uses the IRIG-106 compliant de-randomizer (Modulo 15) in the forward direction)
- Performance: Loop Bandwidth - 0.03% Bit Rate (nominal); Acquisition Range - 1200 ppm Bit Rate; Tracking Range - 1200 ppm Bit Rate
- Output codes: NRZ-L/M/S, BiØ -L/M/S or RNRZ-L. (Note: RNRZ-L uses the IRIG-106 compliant randomizer (Modulo 15) in the Forward direction)
- Serial output: TTL single-ended, RS-422 differential, low voltage differential signaling (LVDS)

Decommutator

- Serial input: TTL Single-ended, RS-422 differential, low voltage differential signaling (LVDS), internal bit sync
- Input codes: NRZ-L or RNRZ-L. (Note: RNRZ-L uses the IRIG-106 compliant derandomizer (Modulo 15) in the forward direction)
- Bits per word: 8 to 16 bits (fixed word size). (Note: Chapter 8, 24 bits per word support by programming to 12 bpw and concatenating 2 words in the Host)
- Bits per minor frame: 8 words to 64K bits
- Minor frames per major frame: 1 to 256 frames
- Minor frame sync bits: 16 to 32 bits
- Minor frame sync mask: 16 to 32 bits
- Search, check and lock errors allowed: 0 to 15 bit errors
- Bit slip window: 0, ±1, ±2, ±3 bits
- Good frames to acquire lock: 1 to 16 frames
- Bad frames to drop lock: 1 to 16 frames
- Major frame sync modes:
  - SFID - Subframe ID Count. Any word in the minor frame.
  - URC - Unique Recycle Code. Any word in the first minor frame.
  - FCC - Frame Code Complement. Minor frame pattern in the first minor frame

Simulator

- Modes: Playback, Fixed Format or PseudoRandom Bit Pattern (PRB Pattern)
- Rate: 30 Kbps to 40 Mbps
- Rate generator: Digital Direct Synthesizer (DDS) in 1 Hz steps or Crystal oscillator in discrete frequencies. Crystal frequency = (80 / N) / 2) MHz, N = 1 to 255 (Note: When DDS generated, the bit synchronizer function is not available)
- Bits per word: 8 to 16 bits. Applies to Playback or Fixed Format
- Data source:
  - Playback - 128 Kword FIFO. Data streamed into the FIFO by Host via the USB port.
  - Fixed Format - 2 Kwords (maximum) SRAM table. Data pre-loaded into the table by Host via the USB port.
  - PRB Pattern - 2^7 - 1 (127 bits), 2^9 - 1 (511 bits), 2^{11} - 1 (2047 bits), 2^{15} - 1 (32767 bits), 2^{20} - 1 (1048575 bits), 2^{23} - 1 (8388607 bits), All ones,
  - All zeros or Dotting (1010)
- Output codes: NRZ-L/M/S, BiØ -L/M/S or RNRZ-L. (Note: RNRZ-L uses the IRIG-106 compliant randomizer (Modulo 15) in the forward direction)
- Serial output: TTL single-ended, RS-422 differential, low voltage differential signaling (LVDS)

Time Code Reader/Generator

- Capability: Elapsed (time starts from 0), Host (Host sets initial time) or IRIG-B Synchronized
- Inputs: Amplitude modulated (AC) or unmodulated (DC) IRIG-B per IRIG-200
- Modulated input: Amplitude modulated signal, single-ended signal levels of 0.5 Vpp up to 10 Vpp and nominal modulation ratio of 3:1
- Unmodulated input: Unmodulated signal, differential, TTL per RS-422
- Acquisition and tracking: Automatically synchronizes to the externally applied input. Will “Flywheel” upon removal of external input and will reacquire upon reapplication of external input
- Internal time base: The internal time base stability over the operating temperature range is ±2ppm during the “flywheel” mode
- Time word formats: Three 16-bit time words are provided. High Time, Low Time and Micro Time. All time word data is per IRIG-106-96 encoding
- Time output: Provides IRIG-B DC output for connection to other equipment
- Time reset: Low active, used only when Elapsed mode is selected. Activating
- “Time Reset” forces the time tags to reset to 0

LEDs

Number: Five (5), Yellow/Green

- Status:
  - + USB activity:
    - › Green, Blinking - Data transfers occurring over the USB port
  - + BitSync lock:
    - › OFF - Disabled
    - › Yellow - Trying to Lock
    - › Green - Locked to the data and recovering Clock
  - + Minor lock:
    - › OFF - Disabled
    - › Yellow - Search
    - › Green - Decommutator Locked to the Minor frame
  - + Major lock:
    - › OFF - Disabled
    - › Yellow - Search
    - › Green - Decommutator Locked to the Major frame
  - + IRIG lock:
    - › OFF - Disabled
    - › Yellow - Trying to Lock
    - › Green - IRIG time code reader Locked to IRIG-B input

Bit Error Rate Tester

- Serial inputs: TTL single-ended, RS-422 differential, low voltage differential signlaing (LVDS), internal bit sync
- Pattern: 2^7 - 1 (127 bits), 2^9 - 1 (511 bits), 2^{11} - 1 (2047 bits), 2^{15} - 1 (32767 bits), 2^{20} - 1 (1048575 bits), 2^{23} - 1 (8388607 bits)
- Synchronization: < 20% errors detected during any 128 bit window
- Error insert: Single, 10^{-1}, 10^{-2}, 10^{-3}
- Error status: Bits received - 32 bit counter, cleared on read. Bits in Error - 32 bit counter, cleared on read

General Purpose Outputs

- Output driver: Two (2) optically isolated outputs, type TLP172A
- Reference: All outputs share a common reference (ISO_ GPO_ RTN)
- Output impedance: 6.0 ohms maximum (in the “ON” condition)
- Maximum current: Up to 40 mA continuous on each output
- Peak off-state voltage: 60 VDC maximum with respect to Digital Ground
- Isolation: 1000 Mohms minimum with respect to Digital Ground
- Logic: The outputs provide a “switch” closure to GPO_ISO_ RTN when activated

General Requirements

- Input voltage: 4.75 VDC to 5.25 VDC, supplied by USB
- Input power: 2.5 Watts nominal
- Grounding: Chassis connected to USB power return
- Operating temperature: 0° to +50°C (box ambient)
- Storage temperature: -20° to +85°C
- Weight: 11.85 oz. (337 grams)
- Dimensions: Basic housing: 5.50” L x 3.00” W x 1.125” H
- Basic housing plus mounting ears and connector protrusion: 6.00” L x 3.75” W x 1.125” H

Ordering Information

DBS-140U-1: USB 2.0 Bit Sync, Decom, Simulator

Included: Programming software application