VPX3-611

Multi-protocol I/O Module

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Key Features

- Advanced I/O options, including MIL-STD-1553B and ARINC 429
- Flexible I/O configurations
- VxWorks® 6.9 SMP drivers
  - \+ Contact factory for additional OS support

Applications

- Military and civil aerospace applications
- SWaP-constrained applications requiring advanced I/O options

Overview

The VPX3-611 I/O module allows customers to readily incorporate a wide variety of I/O into military and aerospace embedded computing systems. Using a simple and reliable Flash-based FPGA hardware architecture with flexible I/O signal routing, the VPX3-611 provides high data throughput performance and can be easily adapted to meet a wide range of application needs.

The VPX3-611 not only fulfills the need for higher integration and flexibility in I/O functionality, but also eases the workload of the processing unit and reduces system production costs through additional processing in the MIL-STD-1553B and ARINC 429 interfaces. As always, this Curtiss-Wright product offers post-purchase technical support, lifecycle management services, and assured long-term availability.

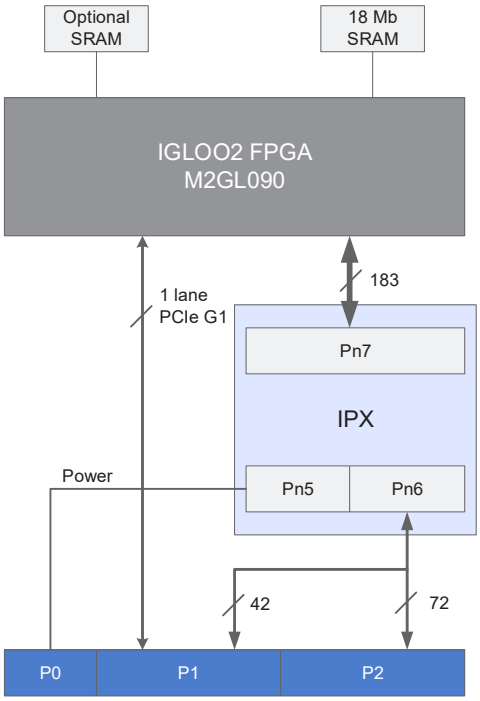

Figure 1: VPX3-611 block diagram

Specification

Form factor

- 3U VPX

I/O capabilities

- MIL-STD-1553B
- ARINC 429
- Asynchronous UARTS
- Discretes
- Up to two I2S analog inputs and two I2S analog outputs
- Serial Peripheral Interface (SPI)
- Others (contact Curtiss-Wright)

Memory

- 18 Mb of SRAM

PCIe

- Interface to the VPX3-611 is through a single lane PCIe Gen1 interface

VITA 65 module profiles

- SLT3-PER-1U-14.3.3
- SLT3-PER-1F-14.3.2

Power

- Designed to meet VITA 46 specifications
- < 15W of power (max)

Software support

- Wind River® VxWorks® 6.9
- Others, please contact Curtiss-Wright

Environmental

Ruggedization

- Conduction-cooled: Level 200

Features

FPGA

At the heart of the VPX3-611 is a Microchip® IGLOO2 M2GL090 FPGA. The FPGA contains the IP implementing all the I/O provided by the VPX3-611. As a Flash-based design, concerns about SEUs are greatly reduced, as well as the startup time for the card.

The FPGA is connected to the VPX3 P1 connector providing a single lane PCIe Gen1 connection to the dataplane. Also connected to the FPGA is 18 Mb of SRAM used as message storage for the 1553 ports. One hundred and eighty-three (183) I/O signals from the FPGA are connected to the IPX Pn7 connector, providing a large amount of I/O conditioning that can be done on the IPX, or that can be passed through to the backplane.

MIL-STD-1553B interfaces

Each MIL-STD-1553B interface supports Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) modes of operation in a dual redundant configuration. The VPX3-611 is compliant to all aspects of MIL-STD-1553B, Notice 2.

Features include:

- BC, RT and BM modes
- Support for auto-response when in BC mode, reducing overhead on CPU and making the VPX3-611 easily integrated with ARINC 653 operating systems
- 18 Mb of SRAM shared per two redundant interfaces, for addition 1553, contact factory

ARINC 429

The VPX3-611 can be configured to provide ARINC 429 TX and ARINC 429 RX channels. Each channel can operate at the high or low bit rates defined by ARINC 429 and can operate concurrently at high speed rates. The VPX3-611 supports message processing to select messages to operate on reducing overhead on CPU.

Serial ports

The VPX3-611 can be configured to provide asynchronous serial channels to the VPX backplane. The serial ports support asynchronous communications with baud rates independently configurable from 1200 to 115200 KBaud.

Discrete Digital I/O (DIO)

The VPX3-611 can be configured to provide independent discrete DIO signals supported from the FPGA.

Digital Audio Interface (I2S)

The VPX3-611 can be configured to provide digital audio interfaces (I2S) inputs and outputs. The outputs can be coupled with internal storage such that the output can be used for audio and provide a pre-recorded warning message for applications such as Helicopter Terrain Avoidance and Warning Systems (HTAWS).

Serial Peripheral Interface (SPI)

The VPX3-611 also provides SPI to enable and simplify program control of system-level functions.

Fabric ports

The VPX3-611 supports PCIe fabric ports to the backplane on P1 as per VITA 46 and VITA 65. The backplane ports are directly connected to the FPGA with the following configuration:

- Single lane PCIe Gen1 port

Temperature sensors

The VPX3-611 provides two temperature sensors to measure board temperatures. The sensors can be read by software.

Safety monitors

The VPX3-611 provides a variety of safety functions to monitor proper board function. Safety Monitors on the VPX3-611 include clock monitors, voltage monitors and temperature monitors.

Interface Personality XMC (IPX)

The Interface Personality XMC (IPX) is based on a standard XMC card format and size. There are three connectors provided on the IPX:

- Pn5 connector is a standard VITA 42 connector and is used to provide power to the IPX if signal conditioning is required.
- The Pn6 connector is a standard VITA 42 connector. All the user I/O from the card is routed from the Pn6 to the P1 and P2 connector.
- The Pn7 connector provides 183 signals from the FPGA to be used by the IPX in providing the required I/O to the backplane.

The IPX can be used to provide the I/O interface conversion and customization in slot - that is, providing the necessary transceivers, transformers, analog conversion, etc., to interface the I/O to external electrical interfaces.

Dependent on the systems needs, Curtiss-Wright can design a custom IPX to suit your systems needs. You can take a simple pass-though module, and provide the drivers received elsewhere in your system.

VPX3-611 provides two types of IPX modules:

1. Passthrough IPX - these IPX modules offer no conditioning of the I/O, and connects the output of the FPGA directly to the backplane. This IPX allows system designer to condition the I/O in the manner or location as they see fit.
2. Conditioned IPX - these IPXs provide conditioning for most of the I/O coming from the FPGA before going to the backplane. This does reduce the number of interfaces available, but in turn the system design does not need to worry about conditioning the I/O.

Conditioned IPX Modules

The VPX3-611 has designed three variants of a conditioned IPX providing various different numbers of I/O depending functional configuration. See Table 6 for available functional configurations. Lightning protection is not provided on the Conditioned IPX. Contact factory for availability.

MIL-STD-1553

The conditioned IPXs can support either transformer coupled or direct coupled interfaces. Table 6 identifies what is supported on a configuration. Due to pin constraints, RTADDRs are not available on IPXs, but a customer specific IPX could be designed to support these if required. Contact factory.

Discrete Digital IO (DIO)

The conditioned IPX can support either LVTTL DIO (input and output), or avionic type I/O (input and output). The IPX is designed to support a maximum of eight LVTTL DIO input and eight DIO output, or four avionic input and four avionic output. Avionic input are current driven input and therefore capable of GND/Open or Supply/Open type of sensing. Avionic input are capable of supporting 35V of input voltage. Avionic output are open drain output and are capable of carrying 200mA.

Serial Ports

The conditioned IPX can support up to eight EIA-232 serial ports or eight EIA-422 async serial ports. The number of serial ports of each type is dependent on the functional configuration. As EIA-422 ports require twice as many signal pairs, other I/O is reduced as a result.

I2S

The conditioned IPX routes I2S TX and I2S RX to the backplane through fet-switches to provide isolation between the backplane and the FPGA. The system design will need to condition these further.

ARINC 429

The conditioned IPX routes the ARINC 429 transmit signals through ARINC 429 drivers and the RX signals through ARINC 429 receivers.

SPI

The conditioned IPX routes both SPIs interfaces to the backplane through fet-switches to provide isolation between the backplane and the FPGA.

Software Support

VPX3-611 drivers are available for VxWorks 6.9. Other software configurations can be supported. Please contact Curtiss-Wright for more details.

Physical Specifications

TABLE 2 Dimensions

OPTION	DIMENSIONS
Conduction-cooled L200	Per VITA 48.1
IPX	5.87 x 2.91” (149 x 74 mm)
RTM3-611	Per VITA 46

TABLE 3 Weight

OPTION	WEIGHT (GRAMS)
Conduction-cooled L200 Mode 1	350
Conduction-cooled L200 Mode 2	360
Conduction-cooled L200 Mode 3/4	<360

Rear Transition Module (RTM)

To gain access to the backplane I/O signals for lab development of the VPX3-611, the RTM3-611 Rear Transition Module is available. Contact factory for RTM support for other IO modes.

TABLE 1 Rear transition module

PART NUMBER	DESCRIPTION
RTM3-611-001	Provides connectors and/or conditioning for the following: › 1 x 1553 (direct-coupled) conditioned › 8 x DIO IN › 8 x DIO Out › 1 x DAC (analog out) › 8 x UARTS › 18/10 x (in/out) ARINC 429 conditioned › 2 x SPI
RTM3-611-002	Provides connectors and/or conditioning for the following: › 1 x 1553 (transformer-coupled) conditioned › 8 x DIO IN › 8 x DIO Out › 1 x DAC (analog out) › 8 x UARTS › 18/10 x (in/out) ARINC 429 conditioned › 2 x SPI
RTM3-611-003	Provides connectors to access › 2 x 1553 (transformer-coupled) › 8 x DIO In Condtioned › 8 x DIO out Condtioned › 2 x DAC and 2 x ADC Analog output and input (analog out) › 8 x EIA-232 ports Condtioned › 18/10 (RX/TX) ARINC 429 Condtioned › 2 x SPI

Power Requirements

TABLE 4 VPX3-611 power requirements

VOLTAGE	COMMENT		
12V (Vs1)	Not used		
3.3V (Vs2)	Only routed to IPX, currently not used		
+3.3VAUX	Only used to pull up backplane system signals and is routed to IPX site		
+/-12VAUX	Not used		
VOLTAGE	RUGGEDIZATION LEVEL	TYPICAL (W)	TYPICAL MAX (W)
5V (Vs3)	Base card - Level 200 Conduction-cooled	1.3	1.6
	IPX 01	0	
	IPX 02	6	
	IPX 03	5.8	
	IPX 04	5.8	

Notes:

1. All power rails defined as in VITA 46.0 for 3U basecards

TABLE 5 RTM3-611 power requirements

UNIT	RUGGEDIZATION LEVEL	TYPICAL (W)	TYPICAL MAX (W)
5V (Vs3)	Level 0 Air-cooled - RTM3-611-001	1.85	
	Level 0 Air-cooled - RTM3-611-002	1.85	
	Level 0 Air-cooled RTM3-611-003, 004, 005	1.2	
3.3V (Vs2)	Not used		
+3.3VAUX	Not used		
12V (Vs1)	Not used		
+/-12VAUX	Not used		

Notes:

1. RTM3-611 is only designed for lab usage in air-cooled chassis.
2. All power rails defined as in VITA 46.0 for 3U RTMs

Ordering Information

The VPX3-611 is ordered with the following part number convention. Please contact Curtiss-Wright for additional configurations.

TABLE 6 Hardware configurations: VPX3-611-uvwyyzz

PART NUMBER	AVAILABLE OPTIONS
Standard prefix for 3U VPX cards	VPX3
Model number	611
u: Cooling method	C: Conduction-cooling
v: Ruggedization	2: Level 200 (-40 to +85°C) 3: Level 200 with covers 9: Customized
w: Mechanical format	1: 0.80” pitch 3: 0.85” pitch, 2-level maintenance covers included 9: Customized
yy: Functional	0: Default 9: Customer specific **Others: Reserved**
zz: Mode	Sequential defined by description See Table 7

Notes:

1. Not all combinations of an orderable variant are available as standard product. Variants highlighted in yellow are standard product.
2. Please consult your local sales office for further help in selecting the appropriate variant.

The following table shows I/O available on variants of the VPX3-611. Other variants will be added as they become available. For more variant options, please contact Curtiss-Wright.

TABLE 7 Functional configuration - VPX3-611-ctmxyzz

MODE zz	1553	DIO IN	DIO OUT	I2S - DAC IN/OUT	UARTS	UART R/CS	429 RX	429 TX	SPI
01 - Passthru	1	8 (L)	8 (L)	1/1	8	0	18	10	2
02 - conditioned	2 (T)	8 (L)	8 (L)	2/2	8 EIA-232	0	18	10	2
03 - conditioned	2 (T)	4 (A)	4 (A)	2/2	8 EIA-422	0	14	8	1
04 - conditioned	2 (T)	4 (A)	4 (A)	1/2	8 EIA-422	0	14	8	2

Notes:

1. (T) - denotes transformer coupled 1553
2. (D) - denotes direct coupled 1553
3. (L) - denotes LVTTL DIO
4. (A) - Avionic Discretes