Chapter 43

Using the KAD/DSI/003/B

TEC/NOT/071

The KAD/DSI/003/B can monitor up to 24 differential or single ended discrete channels. The first eight of these channels can be programmed as special function counters while the remaining 16 channels can be used to trigger time-tagged events.

This technical note describes how to set up the KAD/DSI/003/B, including details of counter settings and event tagging options and is divided into the following sections:

43.1 Physical interface details

The KAD/DSI/003/B has 24 channels, which can be divided into 8 counter channels and 16 trigger time-tagged events. As shown in the following figure, the first eight input channels (channel 0 to channel 7) can be used as programmable counters. See “43.4 Counter channels” on page 3 for further details.

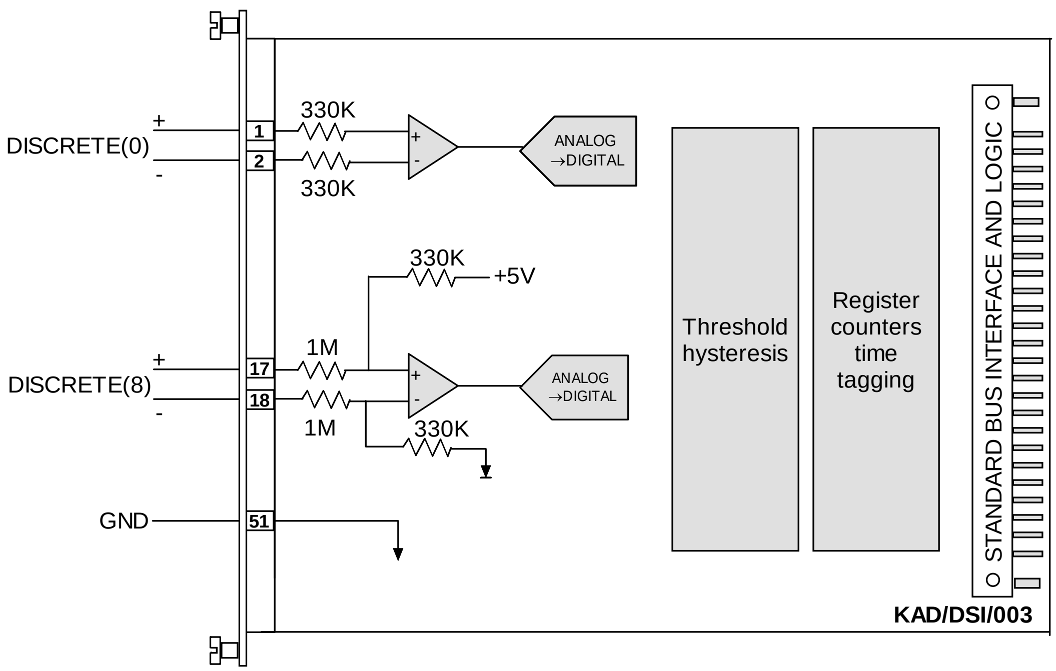


Figure 43-1: First of eight counter inputs and first of sixteen discrete inputs

The remaining 16 channels (channel 8 to channel 23) can be used to trigger time-tagged events and control time tagging to the 8K FIFO (First Input First Output).

43.2 Thresholds and hysteresis

The KAD/DSI/003/B uses upper and lower threshold voltages to achieve hysteresis. Without hysteresis, noisy signals are more prone to create spurious events as shown in the following figure.

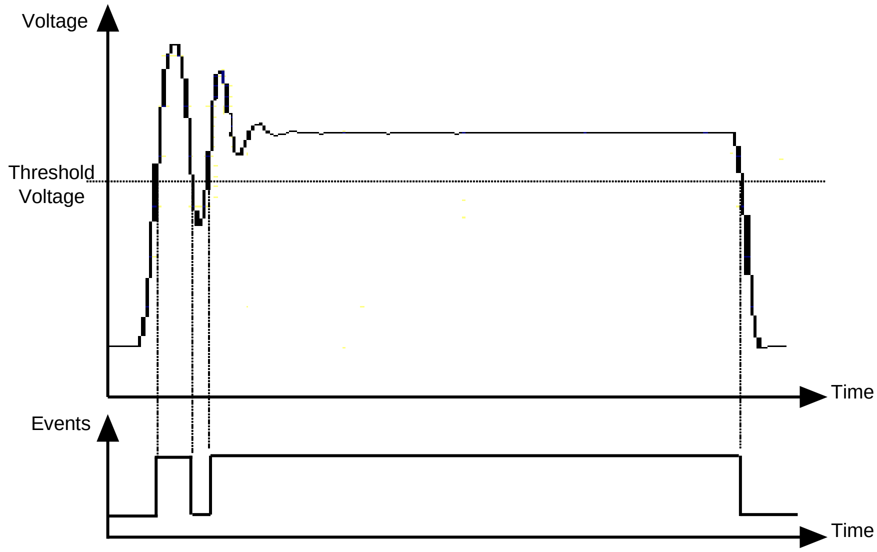


Figure 43-2: Noisy signal creating spurious events

However, by using an upper and lower threshold, these spurious events can be removed as shown in the following figure.

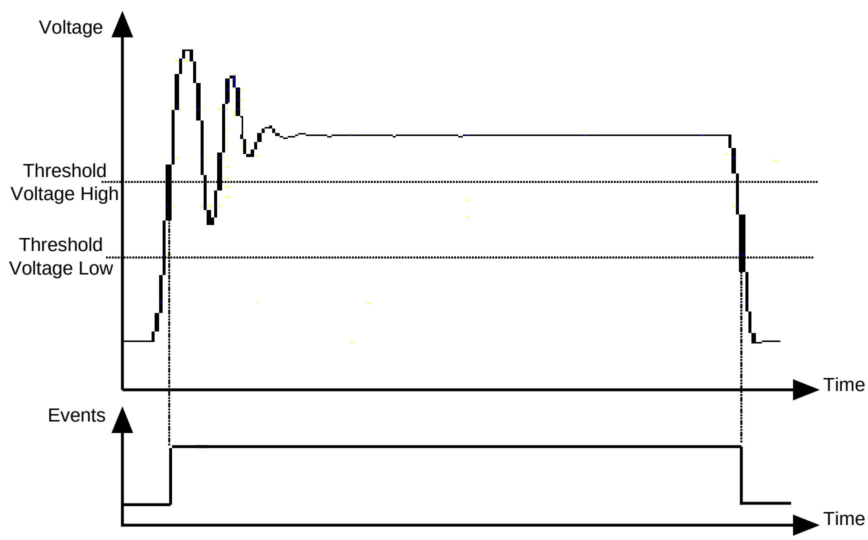


Figure 43-3: Hysteresis prevents spurious events

43.2.1 Event edge detection

When a channel is enabled and thresholds are set by the user, three types of edge detection for events are available: falling, rising, or both. The following figure shows how signal edge detection works.

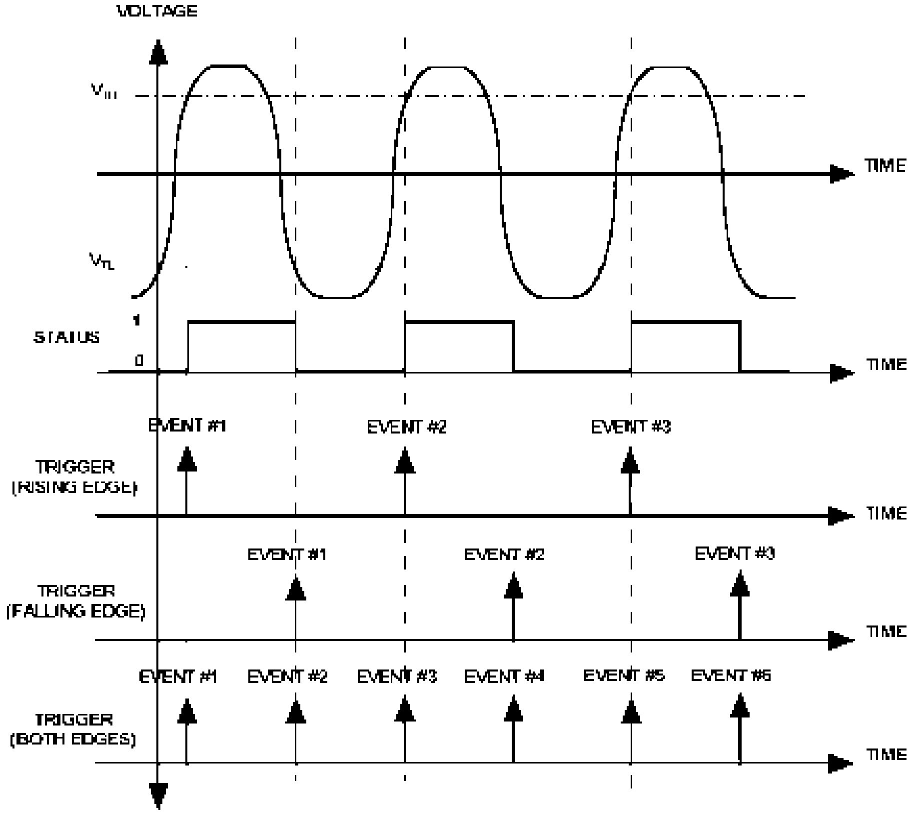


Figure 43-4: Signal edge detection

43.3 Channels 0 to 7 - counter channels

The first eight channels of the KAD/DSI/003/B are connected to special function registers, which can be configured on a channel-by-channel basis.

The frequency range of the counter channels is 0 kHz to 50 kHz. Refer to the *KAD/DSI/003/B* data sheet for further details.

43.3.1 Counter channel interface details

The first 8 channels (channel 0 to 7) have a physical interface as shown in the following figure.

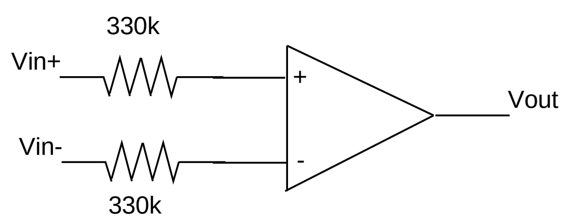


Figure 43-5: Physical interface of channels 0 to 7

The threshold voltages for the counter channels require no special formulas; (V_{out} = V_{in} + - Vin-); desired thresholds are entered into the setup software.

43.3.2 Channels 0 to 7 - Counter channel settings in KSM-500

The following figure shows how the registers for counter channels can be set up in KSM-500.

Parameter Name	Mode	Type	Edge	Setting	Size	Rollover	Threshold Min(V)	Threshold Max(V)
*	*	*	*	*	*	*	*	*
DSI3_0_J5_CNT0_HI	COUNTER_0_HI	PERIOD	Rising	10us	32bit	YES	-10	10
DSI3_0_J5_CNT0_LO	COUNTER_0_LO	PERIOD	Rising	10us	32bit	YES	-10	10
DSI3_0_J5_CNT1_HI	COUNTER_1_HI	FREQUENCY	Rising	1s	32bit	YES	-10	10
DSI3_0_J5_CNT1_LO	COUNTER_1_LO	FREQUENCY	Rising	1s	32bit	YES	-10	10
DSI3_0_J5_CNT2_HI	COUNTER_2_HI	EVENTS_SINCE	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT2_LO	COUNTER_2_LO	EVENTS_SINCE	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT3_HI	COUNTER_3_HI	ELAPSED	Rising	80us	32bit	YES	-10	10
DSI3_0_J5_CNT3_LO	COUNTER_3_LO	ELAPSED	Rising	80us	32bit	YES	-10	10
DSI3_0_J5_CNT4_HI	COUNTER_4_HI	READ	N/A	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT4_LO	COUNTER_4_LO	READ	N/A	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT5_HI	COUNTER_5_HI	EVENTS	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT5_LO	COUNTER_5_LO	EVENTS	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT6_HI	COUNTER_6_HI	RESET	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT6_LO	COUNTER_6_LO	RESET	Rising	N/A	32bit	YES	-10	10
DSI3_0_J5_CNT7_HI	COUNTER_7_HI	PERIOD	Rising	20us	32bit	YES	-10	10
DSI3_0_J5_CNT7_LO	COUNTER_7_LO	PERIOD	Rising	20us	32bit	YES	-10	10

Figure 43-6: DSI/003/B Parameter tab - counter settings in KSM-500

Each counter type has some common settings, which are explained below.

43.3.2.1 Type

Seven counter types are available in KSM-500: PERIOD, FREQUENCY, EVENTS_SINCE, ELAPSED, READ, EVENTS, and RESET.

43.3.2.2 Edge

The counters can be configured to trigger on either Rising or Falling edges of input signals, or Both (rising and falling).

NOTE: In modes such as Frequency mode, the counter Trigger Edge set to Both, results in the values counted being doubled. The Both setting may be desirable when increasing the resolution of the frequency measurement by a factor of two.

43.3.2.3 Setting

Defines the clock period for a counter, if appropriate for the counter type.

43.3.2.4 Size

The counter channels can be 10, 12, 16, 20, 24, or 32 bits wide.

Each counter is divided in two registers with a maximum of 16 bits each: COUNTER_HI and COUNTER_LO.

NOTE: If the size is greater than 16 bits, then the COUNTER_HI register is used in addition to the COUNTER_LO register.

43.3.2.5 Rollover

Determines whether the counter rolls over to zero when the maximum value is reached.

43.3.2.6 Threshold Max and Min

Determines the maximum and minimum threshold which are programmable. Threshold allowable levels are -10V to +10V. Refer to the *KAD/DSI/003/B* data sheet for further details.

43.3.3 Channels 0 to 7 - counter channel settings in DAS Studio 3

With a KAD/DSI/002 module in context, the Settings tab in DAS Studio 3 shows four panes. The following figure shows the pane for programming counter types and thresholds.

Source Name	Counter Type	Threshold Voltage Maximum	Threshold Voltage Minimum	Trigger Edge	Roll Over
Counter(0)	Period	10	-10	Rising	☑
Counter(1)	Frequency	10	-10	Rising	☑
Counter(2)	EventsSinceRead	10	-10	Rising	☑
Counter(3)	Elapsed	10	-10	Rising	☑
Counter(4)	Read	10	-10	Rising	☑
Counter(5)	Events	10	-10	Rising	☑
Counter(6)	Period	10	-10	Rising	☑
Counter(7)	Frequency	10	-10	Rising	☑

Figure 43-7: Counter type settings in DAS Studio 3

Channel 0 to 7 can be programmed with the same settings as KSM-500.

Each counter type has some common settings, which are explained below.

43.3.3.1 Counter Type

Six counter types are available in DAS Studio 3: Period, Frequency, Elapsed, EventsSinceRead, Events, and Read.

NOTE: The *Reset* Counter Type counter is not supported in DAS Studio 3.

43.3.3.2 Threshold Voltage Maximum/Minimum

Determines the maximum and minimum threshold, which are programmable. Threshold allowable levels are -10V to +10V. Refer to the *KAD/DSI/003/B* data sheet for further details.

43.3.3.3 Trigger Edge

The counters can be configured to trigger on either Rising or Falling edges of input signals, or Both (rising and falling).

NOTE: In modes such as Frequency mode, the counter Trigger Edge set to Both, results in the values counted being doubled. The Both setting may be desirable when increasing the resolution of the frequency measurement by a factor of two.

43.3.3.4 Rollover

Determines whether the counter rolls over to zero when the maximum value is reached.

The following figure shows the pane on the Settings tab that is used to program the counter range.

Source Name	Parameter Type	Parameter Name	Range Maximum	Range Minimum
Counter(0)	Counter(0)	P_MyKAD_DSI_003_B_Counter(0)	42949.67296	0
Counter(0)	Counter(0) : CounterLo(0)			
Counter(0)	Counter(0) : CounterHi(0)			
Counter(1)	Counter(1)	P_MyKAD_DSI_003_B_Counter(1)	42949672960	0
Counter(1)	Counter(1) : CounterLo(1)			
Counter(1)	Counter(1) : CounterHi(1)			
Counter(2)	Counter(2)	P_MyKAD_DSI_003_B_Counter(2)	4294967296	0
Counter(2)	Counter(2) : CounterLo(2)			
Counter(2)	Counter(2) : CounterHi(2)			
Counter(3)	Counter(3)	P_MyKAD_DSI_003_B_Counter(3)	42949.67296	0
Counter(3)	Counter(3) : CounterLo(3)			
Counter(3)	Counter(3) : CounterHi(3)			
Counter(4)	Counter(4)	P_MyKAD_DSI_003_B_Counter(4)	4294967296	0
Counter(4)	Counter(4) : CounterLo(4)			
Counter(4)	Counter(4) : CounterHi(4)			
Counter(5)	Counter(5)	P_MyKAD_DSI_003_B_Counter(5)	4294967296	0
Counter(5)	Counter(5) : CounterLo(5)			
Counter(5)	Counter(5) : CounterHi(5)			
Counter(6)	Counter(6)	P_MyKAD_DSI_003_B_Counter(6)	42949.67296	0
Counter(6)	Counter(6) : CounterLo(6)			
Counter(6)	Counter(6) : CounterHi(6)			
Counter(7)	Counter(7)	P_MyKAD_DSI_003_B_Counter(7)	42949672960	0
Counter(7)	Counter(7) : CounterLo(7)			
Counter(7)	Counter(7) : CounterHi(7)			

Figure 43-8: Counter range settings in DAS Studio 3

In DAS Studio 3, the registers for the counter channels are by default 32 bits and—as many other registers bigger than 16 bits—can be optionally split into 2 x 16-bit registers called Counter_HI and Counter_LO. If only Counter_LO is transmitted, the counter size is automatically set to 16 bits, whereas if the full 32-bit counter is transmitted, DAS Studio 3 sets the counter size to 32 bits.

In DAS Studio 3, setting up a clock frequency is not required; allowed frequency ranges are automatically displayed.

The Maximum and Minimum range settings in this block are chosen from a drop-down menu, while values are predetermined by the counter type (such as frequency and period) used in the previous section of this document. The frequency counter range is expressed in Hertz, while period counter is expressed in seconds.

Some Counter types such as Read have no Max/Min range settings. The following section explains how the values available in the range's drop-down menus are calculated.

43.4 Counter types

43.4.1 Counting events – Frequency counter

In Frequency mode operation, the number of events in a specified time interval are counted.

The formula to calculate the input frequency is:

$$Fin = counts \times F\_clk$$

Proper use of the Frequency and Period counters can maximize the resolution of the measurement being undertaken. As a general rule, Period is used for slower signals and Frequency for faster signals.

The sampling rate for Period and Frequency counters is only relevant for monitoring purposes. The sampling rate should be high enough to ensure that any event can be observed, while the maximum update rate is 1 Hz.

43.4.1.1 Example of Frequency counter in KSM-500

Refer to the following table for Frequency counter settings.

Type	Edge	Setting	Size	Fs (sampling frequency)
FREQUENCY	RISING	1 second	16 bits	1000 sps

Measuring input frequency of (F_{in}) = 100 Hz

In this case, events that occur at 100 Hz (10 ms) are counted for a duration of 1s.

Hence 100 counts result in: (F_{in} = 100 / Flck = 1 sec)

43.4.1.2 Frequency counter settings in DAS Studio 3

In DAS Studio 3, the Frequency counter is fixed at 32 bits and offers five ranges which correspond to the following clock setting intervals.

Module level setting		DAS Studio 3 setting			
Type	**Interval setting**	**Required unit**	**Bits**	**Max range**	**Min range**
FREQUENCY	100 ms	HERTZ	32	42949672960	0
	250 ms	HERTZ	32	17179869184	0
	500 ms	HERTZ	32	8589934592	0
	1s	HERTZ	32	4294967296	0
	2s	HERTZ	32	2147483648	0

A range of 2147483648 (2 seconds internal clock setting) offers the best resolution with 2 counts/Hertz making it a suitable counter for high frequency signals.

43.4.2 Counting events – Events counter

In the EVENTS mode of operation, the EVENTS register increments every time an event occurs and rolls over.

There is no clock setting required for the EVENTS mode of operation.

43.4.2.1 Example of Events counter in KSM-500

Refer to the following table for Events counter settings.

Type	Edge	Setting	Size	Fs (sampling frequency)
EVENTS	RISING	N/A	16 bits	1000 sps

Measuring input frequency of (F_{in}) = 100 Hz

The EVENTS register increments every time an event occurs, in this case at 100 Hz.

Expected output = output incrementing at 100 counts/second

43.4.2.2 Events counter settings in DAS Studio 3

There are no range settings in DAS Studio 3.

43.4.3 Counting events – Events_Since counter

In the EVENTS_SINCE mode of operation, all events are counted since the EVENTS_SINCE register was last read. In other words, when EVENTS_SINCE is read, the register resets it to 0, and then it increments every time an edge is detected until it is read again.

The formula to calculate the input frequency is:

F_in = counts x Fs

43.4.3.1 Example of EVENTS SINCE counter in KSM-500

Refer to the following table for EVENTS SINCE counter settings.

Type	Edge	Setting	Size	Fs (sampling frequency)
EVENTS_SINCE	RISING	N/A	16 bits	1000 sps

Measuring input frequency of (Fin) = 10 kHz

In this case, the EVENTS SINCE register is read at F_S = 1000 sps (1 ms = 1000 µs). With events occurring at 10 kHz (100 µs), the EVENTS SINCE register reads 10 counts.

43.4.3.2 Events since counter/EventsSinceRead settings in DAS Studio 3

In DAS Studio 3, this register is called EventsSinceRead and has the following fixed range settings.

Module level setting		DAS Studio 3 setting			
Type	**Interval setting**	**Required unit**	**Bits**	**Max range**	**Min range**
EVENTS_SINCE	N/A	COUNTS	32	4294967296	0

43.4.4 Counting time – Period counter

In the PERIOD counter mode of operation, an internal clock measures the time (clock ticks) between events and returns the number of clock ticks between edges.

The Period counter is typically used for measuring relatively low frequency pulse trains (for example, the 1pps output of a GPS).

The formula to calculate the input period is:

Pin = counts x P_clk

43.4.4.1 Example of PERIOD counter in KSM-500

Refer to the following table for PERIOD counter settings.

Type	Edge	Setting	Size	Fs (sampling frequency)
PERIOD	RISING	10 µs	16 bits	1000 sps

Measuring input frequency of 100 Hz (PERIOD = 10 ms)

In this case, events occur at 100 Hz (10 ms) while the time between events is measured in units of 10 µs.

Hence 1000 counts are expected (P_{in} = 10 ms / Plck = 0.01 ms)

43.4.4.2 Period counter settings in DAS Studio 3

In DAS Studio 3, the Period counter is fixed at 32 bits and offers four ranges, which correspond to the following clock setting intervals.

Module level setting		DAS Studio 3 setting			
Type	**Interval setting**	**Required unit**	**Bits**	**Max range**	**Min range**
PERIOD	10 µs	SECONDS	32	42949.67296	0
	20 µs	SECONDS	32	85899.34592	0
	40 µs	SECONDS	32	171798.6918	0
	80 µs	SECONDS	32	343597.3837	0

43.4.5 Counting time – ELAPSED

In the ELAPSED mode of operation, an internal clock measures the time between the last event and the current read of the ELAPSED register. In other words, the value of this register represents the number of ticks between samples.

NOTE: The EVENTS_SINCE and ELAPSED counters can be used to measure acceleration.

43.4.5.1 Example of ELAPSED counter in KSM-500

Refer to the following table for ELAPSED counter settings.

Type	Edge	Setting	Size	Fs (sampling frequency)
ELAPSED	RISING	10 µs	16 bits	1000 sps

Measuring input frequency of (Fin) = 10 kHz

In this case, events occur at 10 kHz (100 µs). Hence the time between the last event and the current read of the ELAPSED register is 0 to 100 µs. As the duration is measured in increments of 10 µs, then the ELAPSED register reads anything between 0 and 10.

Expected Output = a value between 0 and 10 counts

43.4.5.2 Elapsed settings in DAS Studio 3

In DAS Studio 3 the ELAPSED counter is fixed at 32 bits and offers four ranges, which correspond to the following clock setting intervals.

Module level setting		DAS Studio 3 setting			
Type	**Interval setting**	**Required unit**	**Bits**	**Max range**	**Min range**
ELAPSED	10 µs	SECONDS	16	0.65536	0
	20 µs	SECONDS	16	1.31072	0
	40 µs	SECONDS	16	2.62144	0
	80 µs	SECONDS	16	5.24288	0

43.4.6 Counting samples – Read

This counter increments every time it is sampled. There are no software settings for this register.

NOTE: The Read counter is useful in a telemetry application in a PCM frame as a minor frame counter. For example, if a 32-bit READ counter is read once per 1 ms major frame, then it can act as a major frame counter that cycles every 49.7 days (= 232 × 1 ms).

43.4.7 Counting samples - Event with Reset counter (KSM-500 only)

This counter acts as a reset input to the next counter. On detection of an event, the RESET counter increments and resets the next counter to 0. Channels 0, 2, 4, and 6 can be configured as Reset counters meaning that an event on a Reset channel resets the counter on the next channel. To do this, the next counter must be set to EVENT type.

For example:

- Reset Event on Channel 0 increments Counter 0 and resets Counter 1
- Reset Event on Channel 2 increments Counter 2 and resets Counter 3
- Reset Event on Channel 4 increments Counter 4 and resets Counter 5
- Reset Event on Channel 6 increments Counter 6 and resets Counter 7

There is no setting required for the RESET mode of operation.

The following figure shows the effect of a Reset counter on channel 0 configured for a rising edge trigger on a Read counter on channel 1.

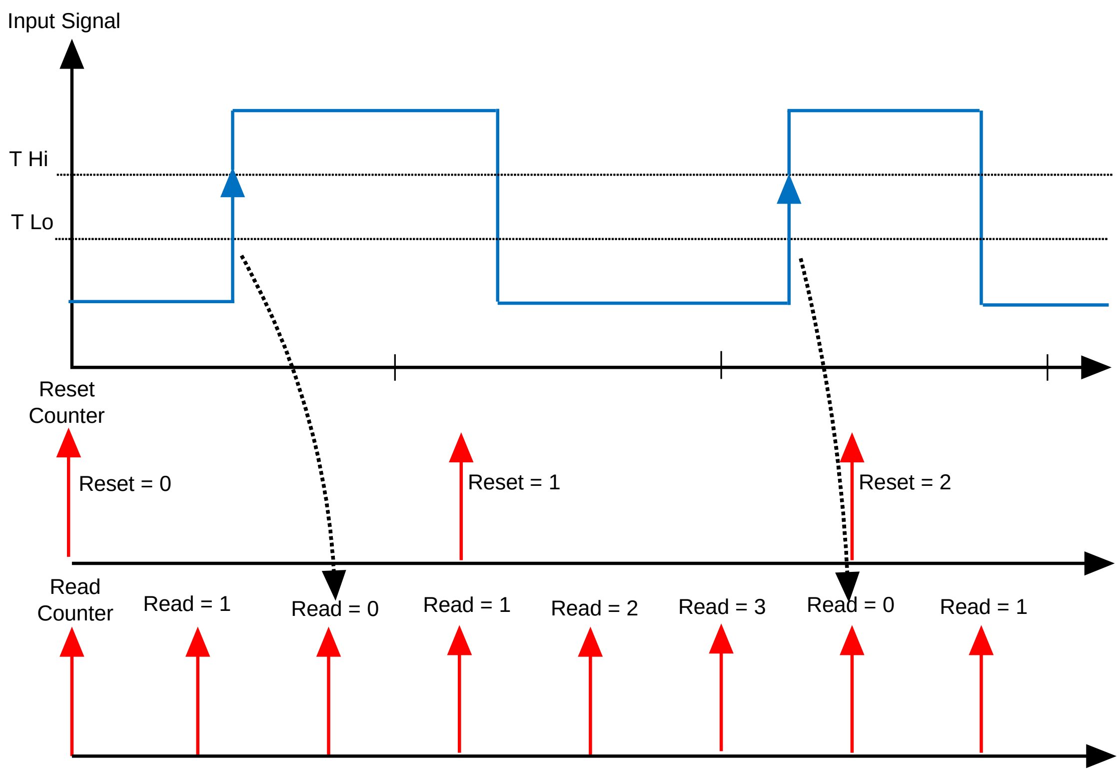


Figure 43-9: Sample operation of the Reset counter

NOTE: The RESET counter is implemented in KSM-500 only.

43.5 Discrete channels

Channels 8 through 23 of the KAD/DSI/003/B are discrete channels, which are used to measure simple on/off events. These events can be time tagged with microsecond time and sent to an 8K word FIFO for subsequent reading.

The TAG_EVENT_STATUS register gives the status of the 16 discrete channels at a particular instant in time.

43.5.1 Discrete channel interface details

The last 16 channels (channel 8 to 23) have a physical interface as shown in the following figure.

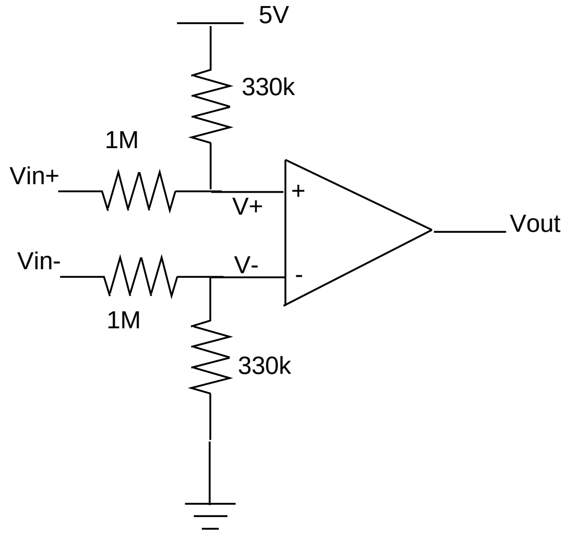


Figure 43-10: Physical interface of channels 8 to 23

43.5.1.1 Setting discrete channel threshold voltages

The required threshold voltages (Vout) can be calculated as follows:

The output value is: Vout = V(+) - V(-)

$$V_{+} = \frac{(V_{in+} * 330k\Omega + 5 * 1M\Omega M}{1M\Omega + 330k\Omega}$$

$$V- = \frac{(V_{in-} * 330k\Omega 3}{1M\Omega + 330k\Omega}$$

$$V_{out} = Vth = V_{+} - V_{-} = \frac{(V_{in+} - V_{in-}) * 330k\Omega}{1330k\Omega} + 5 * \frac{1000k\Omega}{1330k\Omega}$$

43.5.1.2 Floating Inputs Counter channels - Ch 0 to Ch 7

As per Figure 43-5 on page 3, floating Inputs on these channels could be pulled to either rail.

43.5.1.3 Inputs Discrete channels - Ch 8 to Ch 23

With DISCRETE(+) disconnected, then V+ is pulled to +5V.

With DISCRETE(-) disconnected, then V- is pulled to GND.

In order to achieve floating inputs to give logic 0, the threshold values must be set as follows:

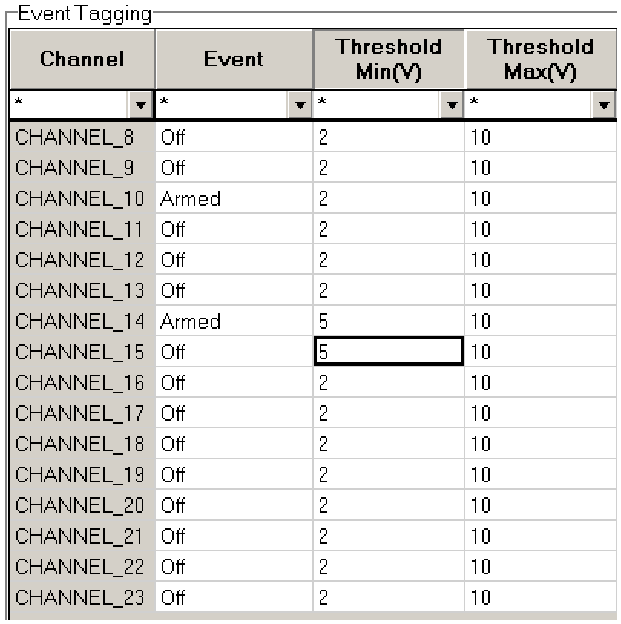
5.5V < VTHL < 10V

VTHL < VTHH

See “43.6 Discrete channel wiring options” on page 15 for further details on wiring options.

43.5.2 Channels 8 to 23 - discrete channel settings in KSM-500

The following figure illustrates the setup of the KAD/DSI/003/B discrete channels (Ch8 to Ch23) in KSM-500.



Event Tagging

Channel	Event	Threshold Min(V)	Threshold Max(V)
*	*	*	*
CHANNEL_8	Off	2	10
CHANNEL_9	Off	2	10
CHANNEL_10	Armed	2	10
CHANNEL_11	Off	2	10
CHANNEL_12	Off	2	10
CHANNEL_13	Off	2	10
CHANNEL_14	Armed	5	10
CHANNEL_15	Off	5	10
CHANNEL_16	Off	2	10
CHANNEL_17	Off	2	10
CHANNEL_18	Off	2	10
CHANNEL_19	Off	2	10
CHANNEL_20	Off	2	10
CHANNEL_21	Off	2	10
CHANNEL_22	Off	2	10
CHANNEL_23	Off	2	10

Figure 43-11: Discrete Channel set up in KSM-500

The discrete channels have the following settings:

43.5.2.1 Event

This setting enables/disables a discrete channel. Each channel can be Armed or Off.

NOTE: Ensure that unused inputs are disabled in order to avoid FIFO overflows due to undesired events when using time tagging events. See “43.7 Using the event FIFO” on page 18 for further details.

43.5.2.2 Maximum/Minimum Threshold Voltage

The maximum/minimum threshold voltage allowed for channels 8 to 23 is -55V to 25V respectively.

Refer to the *KAD/DSI/003/B* data sheet for further details.

43.5.3 Channels 8 to 23 - Discrete channel settings in DAS Studio 3

The following figure illustrates the setup of the KAD/DSI/003/B discrete channels (Ch8 to Ch23) in DAS Studio 3.

Source Name	Event Armed	Threshold Voltage Maximum	Threshold Voltage Minimum
Discrete(8)	☐	10	2
Discrete(9)	☐	10	2
Discrete(10)	☐	10	2
Discrete(11)	☐	10	2
Discrete(12)	☐	10	2
Discrete(13)	☐	10	2
Discrete(14)	☐	10	2
Discrete(15)	☐	10	2
Discrete(16)	☐	10	2
Discrete(17)	☐	10	2
Discrete(18)	☐	10	2
Discrete(19)	☐	10	2
Discrete(20)	☐	10	2
Discrete(21)	☐	10	2
Discrete(22)	☐	10	2
Discrete(23)	☐	10	2

Figure 43-12: Discrete Channel setup in DAS Studio 3

The discrete channels have the following settings:

43.5.3.1 Event/Event Armed

This setting enables/disables a discrete channel.

43.5.3.2 Maximum/Minimum Threshold Voltage

The maximum/minimum threshold voltage allowed for channels 8 to 23 is -55V to 25V respectively.

43.5.3.3 Event status and event time tagging

The 16 discrete channels (channel 8 to channel 23) control the time tagging to the 8K FIFO. For each armed (enabled) channel, time tagging can be triggered by an event.

Every time a trigger occurs, a 64-bit event status word that contains the microsecond timestamp of the event, is written to the FIFO.

This timestamping consists of a 48-bit register for time tagging and a 16-bit register to track the state of the 16 discrete inputs (after the change of state). The time tag is the Binary Coded Decimal (BCD) time of when the event happened (up to 23 hours 59 minutes 59.99 9999 seconds).

43.5.4 Channels 0 to 23 discrete status with time tagging in KSM-500

All 24 discrete signals corresponding to channel 0 to 23 can be read as a 24-bit words (16-bit + 8-bit or 12-bit + 12-bit).

The discrete channels have common settings, which are explained in the following figure and the table thereafter.

Parameter Name	Mode	Type	Edge	Setting	Size	Rollover	Threshold Min(V)	Threshold Max(V)
*	*	*	*	*	*	*	*	*
DSI3_ST_LO_12B0_J6	Status_11_0	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_ST_LO_16B0_J6	Status_15_0	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_ST_HI_12B0_J6	Status_23_12	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_ST_HI_8B0_J6	Status_23_16	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_EV_0_J6_STATUS	TAG_EVENT_STATUS	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_EV_0_J6_HI	TAG_EVENT_TIME_HI	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_EV_0_J6_LO	TAG_EVENT_TIME_LO	N/A	N/A	N/A	N/A	N/A	N/A	N/A
DSI3_EV_0_J6_MICRO	TAG_EVENT_TIME_MICRO	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Figure 43-13: Discrete status parameters with time tagging in KSM-500

The following STATUS registers are available.

Register name	Bits	Description
DSI3_ST_HI_12B0_Jx	16	Bit 4 to bit 15 monitors the status (high/low) of channel 12 to channel 23.
DSI3_ST_LO_12B0_Jx	16	Bit 0 to bit 11 monitors the status (high/low) of channel 0 to channel 11.
DSI3_ST_HI_8B0_Jx	16	Bit 8 to bit 15 monitors the status (high/low) of channel 16 to channel 23. Note: This register is padded with eight 0s on the LSB side.
DSI3_ST_LO_16B0_Jx	16	Bit 0 to bit 15 monitors the status (high/low) of channel 0 to channel 15.

NOTE: The 12 + 12 or 16 + 8-bit distribution represents the same information and is supported under KSM-500 due to legacy reasons. All registers can be used at the same time.

Event related registers with timestamp are explained in the following table.

Register name	Bits	Description
DSI3_EV_0_Jx_STATUS	16	Bit 0 to bit 15 monitors the status (high/low) of channel 8 to channel 23. When the FIFO is empty the last values are repeated.
DSI3_EV_0_Jx_HI	16	Hours and minutes of the timestamp associated with the DSI3_EV_0_Jx_STATUS event. Refer to the *KAD/DSI/003/B* data sheet for further details.
DSI3_EV_0_Jx_LO	16	Centiseconds and seconds of the timestamp associated with the DSI3_EV_0_Jx_STATUS event. Refer to the *KAD/DSI/003/B* data sheet for further details.
DSI3_EV_0_Jx_MICRO	16	Microseconds of the timestamp associated with the DSI3_EV_0_Jx_STATUS event. Refer to the *KAD/DSI/003/B* data sheet for further details.

NOTE: The EVENT TAG register is a 64-bit register split into 4 x16-bit registers above which coherency is guaranteed.

43.5.5 Channels 0 to 23 discrete status with time tagging in DAS Studio 3

The discrete channels have common settings, which are explained in the following figure and the table thereafter.

Parameter Type	Parameter Name
TagIrigTime48	*P_KAD_DSI_003_B_0_TagIrigTime48*
TagIrigTime48 : TagTimeHi	
TagIrigTime48 : TagTimeLo	
TagIrigTime48 : TagTimeMicro	
TagStatus	*P_KAD_DSI_003_B_0_TagStatus*
Discrete	*P_KAD_DSI_003_B_0_Discrete*
Discrete : DiscreteHi	
Discrete : DiscreteLo	

Figure 43-14: Discrete status parameters with time tagging in DAS Studio 3

Event related registers with timestamp are explained in the following table.

Register name	Bits	Description
TagIrigTime48	48	Time stamp with microsecond resolution of the timestamp associated with the register TagStatus. Contains TagTimeHi + TagTimeLo + TagTimeMicro. This is equivalent to DSI3_EV_HI, DSI3_EV_LO and DSI3_EV_MICRO referred to DSI3_EV_STATUS in KSM-500.
TagIrigTime48:TagTimeHi	16	Hours and minutes of the timestamp associated with the register TagStatus. This is equivalent to DSI3_EV_HI in KSM-500.
TagIrigTime48:TagTimeLo	16	Seconds and centiseconds of the timestamp associated with the register TagStatus. This is equivalent to DSI3_EV_LO in KSM-500.
TagIrigTime48:TagTimeMicro	16	Microseconds of the timestamp associated with the register TagStatus. This is equivalent to DSI3_EV_MICRO in KSM-500.
TagStatus	16	Bit 0 to bit 15 monitors the status (high/low) of channel 8 to channel 23. When the FIFO is empty the last values are repeated. This is equivalent to DSI3_EV_STATUS in KSM-500.
Discrete	32	The values of the 24 discrete inputs labeled 23 down to 0. Bit 0 to bit 15 monitors the status (high/low) of channel 0 to channel 15. Bit 24 to bit 31 monitors the status (high/low) of channel 16 to channel 23. Contains the same information as DiscreteHi + DiscreteLo.
DiscreteHi	16	Bit 8 to bit 15 monitors the status (high/low) of channel 16 to channel 23.
DiscreteLo	16	Bit 0 to bit 15 monitors the status (high/low) of channel 0 to channel 15.

43.6 Discrete channel wiring options

For single ended signals, connect to the positive input for each channel. The negative input can be left floating, however it is recommended to tie it to ground (GND).

The following examples illustrate some uses of the KAD/DSI/003/B discrete channels.

43.6.1 Detecting a 28V/open signal

The KAD/DSI/003/B discrete channels can be configured to read a 28V/open discrete signal as shown in the following figure.

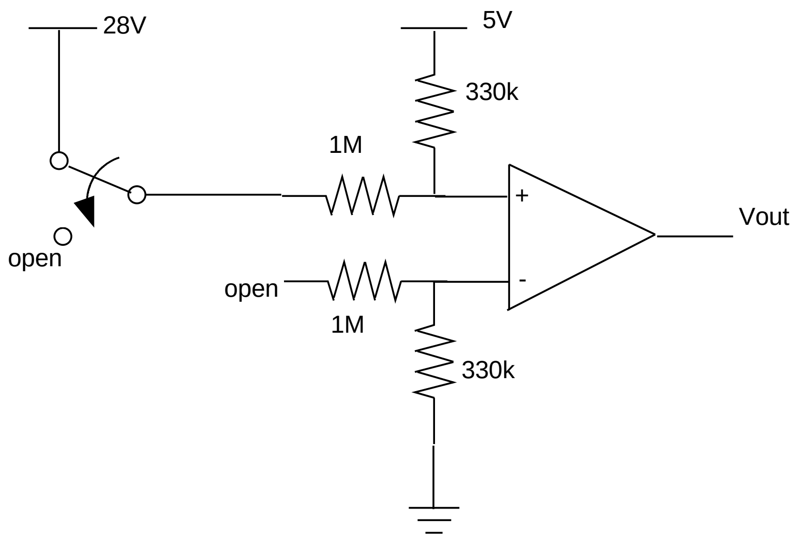


Figure 43-15: Configuration for detecting a 28V/open signal

With the Vin- input left floating, the input to the comparator is pulled to GND.

When the Vin+ input is switched to 28V, the input to the comparator is 10.71V. When the Vin+ input is left in the open position, then the input to the comparator is 5V.

The midpoint between these two values is 4.38V, therefore the minimum lower transition should be 4.07V and the maximum upper transition should be 4.69V. That is, in the setup GUI, a minimum threshold of 4.2V and a maximum threshold of 4.6V is reasonable.

43.6.2 Detecting 28V/GND signal

The KAD/DSI/003/B discrete channels can be configured to read a 28V/GND discrete signal as shown in the following figure.

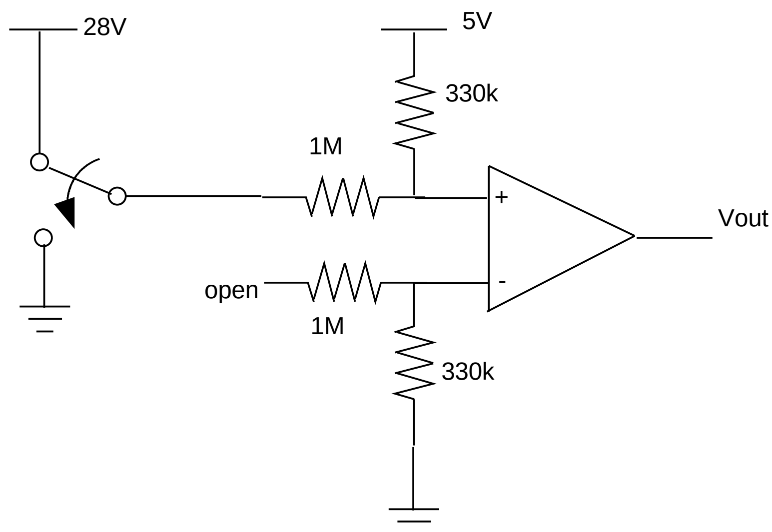


Figure 43-16: Configuration for detecting a 28V/GND signal

With the Vin- input left floating, the input to the comparator is pulled to GND.

When the Vin+ input is switched to 28V, the input to the comparator is 10.71V. When the Vin+ input is switched to the GND position, then the input to the comparator is 3.76V.

The midpoint between these two values is 7.235V, therefore the lower threshold should be 7V and the upper transition should be 7.5V.

43.6.3 Detecting GND/Open signal

The KAD/DSI/003/B discrete channels can be configured to read a GND/Open discrete signal as shown in the following figure.

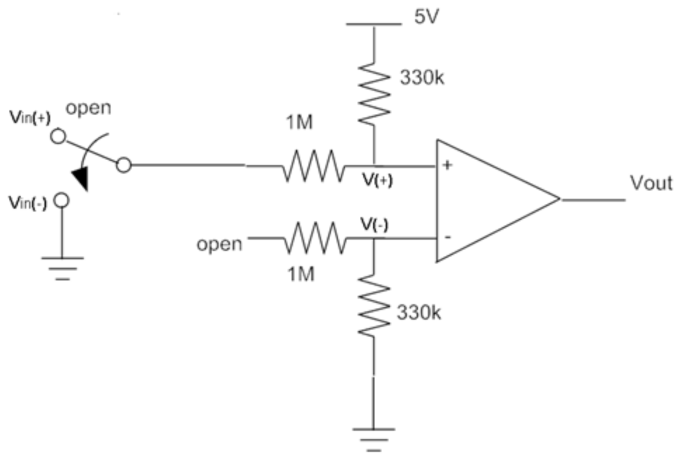


Figure 43-17: Figure 65-16: Configuration for detecting an Open/GND signal

Assuming that Vin- is left opened and Vin+ toggles between GND and open, then V- is pulled to GND.

When the switch is pulled to GND, V+ follows the equation shown in "43.5.1 Discrete channel interface details" on page 11, giving V+ = 3.76.

When the switch is opened then V+ is pulled to 5V.

The midpoint between these two values is 4.38 V, therefore the lower threshold should be 4.07V and the upper transition should be 4.69V.

43.7 Using the event FIFO

If a discrete channel is Armed, then when an event occurs on that channel it is sent to the FIFO. The following figure illustrates the relationship between events, the FIFO, and sampling.

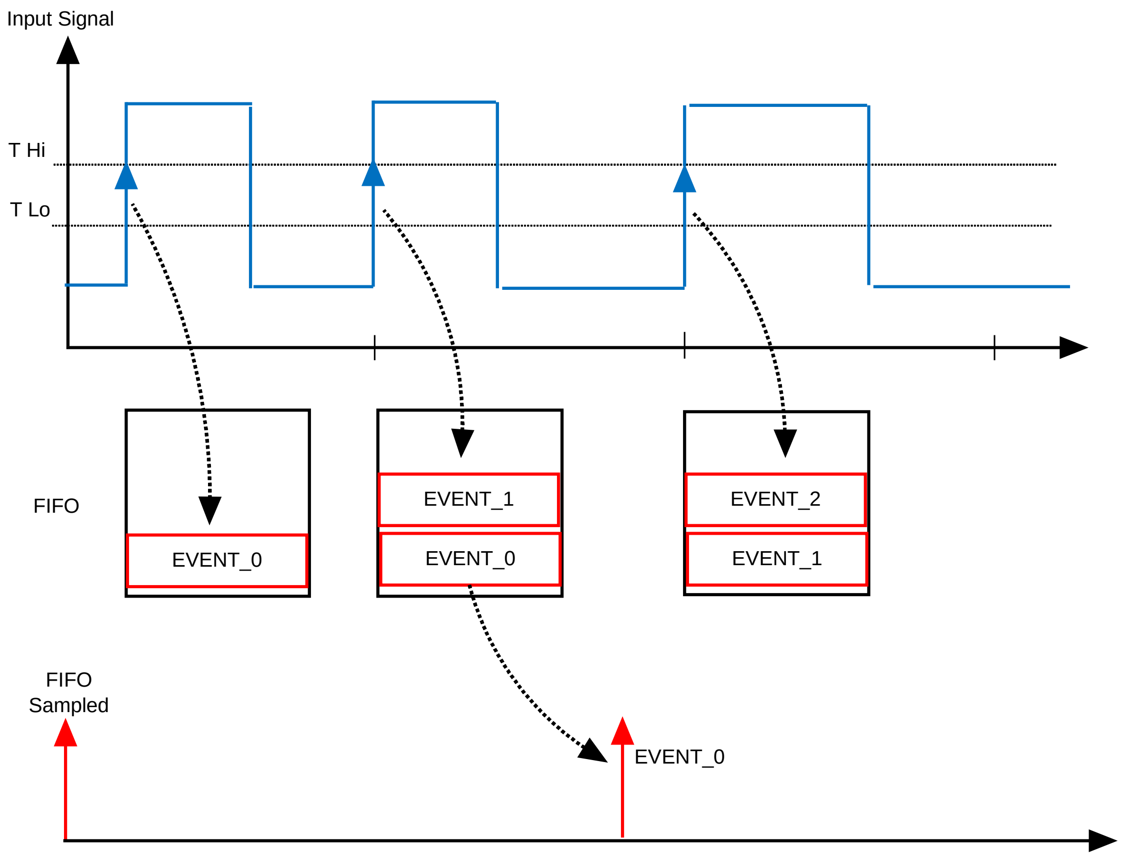


Figure 43-18: Events and the FIFO

NOTE: Each of the 64-bit registers associated with tagging (Event_Status, Event_Time_Hi, Event_Time_Lo, and Event_-Time_Micro) has its own dedicated 8K word buffer. This means that the FIFO buffer can fill if 8192 events occur between reads. To avoid this situation, the FIFO should be read so that the sampling speed at least equals the frequency of the incoming signals.

43.8 Choosing the correct counter mode

The frequency of an input signal can be measured in two ways:

Measure PERIOD and invert in Groundstation (Real Time or Post Processing)

Measure FREQUENCY over a defined period of time

FREQUENCY counter is directly calculated on the module over a defined time period and it is used to measure high frequency signals. The PERIOD counter provides poor resolution at high frequencies as the fastest clock for the PERIOD counter is 10 µs.

For example, at 50 kHz the PERIOD counter shows 1 count, while at 33 kHz the PERIOD counter shows 3 counts. However the PERIOD counter provides excellent resolution at low frequencies. For example, at 2 Hz, the PERIOD counter shows 50000 counts and at 2.01 Hz the PERIOD counter shows 49751 counts.

As a rule of thumb and depending on the resolution required, FREQUENCY counter mode provides better results for frequencies greater than 1 kHz, while PERIOD counter mode is recommended for frequencies lower than 1 kHz.

NOTE: The maximum update rate for the frequency counter is 1 Hz. Newer modules such as the KAD/DSI/102 support a maximum update rate of 10 Hz for the frequency counter.

43.9 Related documentation

DOCUMENT	DETAILS
DOC/DBK/001	Acra KAM-500 Databook
DOC/MAN/018	KSM-500 Databook
DOC/MAN/030	DAS Studio 3 User Manual
DST/N/091	KAD/DSI/003/B data sheet

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