RBDS-120

RF Receiver, Bit Sync, Decom, Simulator and IRIG Time Code Reader

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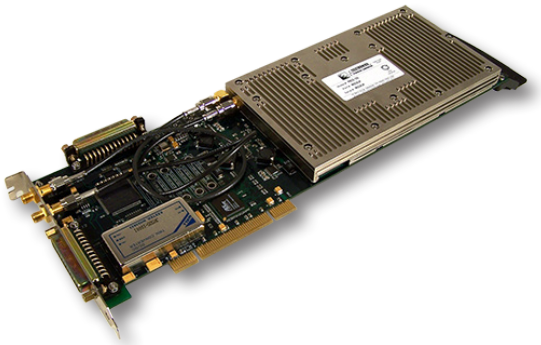


Key Features

- PC-based PCI bus full size card with RF receiver, bit synchronizer, data decommutator, simulator, and IRIG time code reader
- RF receiver
  - L band or S band coverage
  - Selective tuning with 20 kHz tuning steps
  - 4 selectable IF band widths; 0.5 to 20 MHz available
- Bit sync
  - Bit rates up to 10 Mbps, NRZ Codes
  - Input signal amplitudes from 0.1 to 5.0Vp-p
- Data decommutator
  - PCM input rate up to 20 Mbps
  - Accepts RS-422 or TTL input data and clock
- Microsoft® Windows® compatible driver software included
- Supported by third party data analysis software

Applications

- Data analysis
- Data archival
- Flight test instrumentation

Overview

The RBDS-120 combines the functions of RF receiver, bit synchronizer, data decommutator and simulator into a single full size PCI bus card. The card can be installed in a desk top PC for preflight or lab test. The RF receiver has L or S band coverage (customer specified at time of order). Tuning is in 20Khz steps. There are four selectable IF bandwidths from 0.5MHz to 20MHz. The bit synchronizer provides full-featured clock reconstruction, data recovery and code conversion. The bit sync accepts PCM inputs at rates of up to 10 Mbps for NRZ codes and up to 5 Mbps for BiØ codes with amplitudes from 0.1 to 5.0 Volts p-p. The bit sync input impedance is programmable to 50, 75 or 10K ohms. PCM data and 0°/180° clock bit sync outputs are provided via RS422 and TTL drivers. The bit sync output is also internally connected to the on card decom. A Bit Error Rate (BER) measurement capability with an on card test data simulator is included to allow characterization of data link quality. The data decommutator provides full IRIG frame synchronization and data decommutation. The decom accepts PCM data at rates up to 20 Mbps from either an external source or the on-card bit sync (10 Mbps max.). The decom external data and clock inputs are programmable for RS-422 (20 Mbps–120 ohm) or TTL (10 Mbps–10K ohm). Decommutated data words and frame time tags are made available via the PCI bus for analysis, archival, and monitoring. The card also features a playback mode. In this mode the card regenerates archived PCM data at programmable rates up to 20 Mbps. A parallel output port provides the customer with the frame data and control signals. The customer can cherry pick any or all desired words from the frame. A DB25 connector is used for each the parallel output port (top of card) and the I/O port (rear of card on rear I/O plate). The rear I/O plate is also equipped with two SMA connectors, one for the RF receiver input (antenna) and one for the analog/TTL direct bit sync input.

Additional Features

- Simulator
  - Regenerates playback archived PCM data at programmable rates of up to 20 Mbps
  - Random number generator: Used for checking bit sync
- IRIG-B time code reader
  - Accepts IRIG AC or DC time in
  - Time tags incoming PCM minor frames
  - Provide IRIG Time to the PC

RF Receiver

- RF tuning range:
  - Lower L-Band (1430 to 1540 MHz)
  - Upper L-Band (1710 to 1850 MHz)
  - Lower S-Band (2200 to 2300 MHz)
  - Upper S-Band (2300 to 2400 MHz)
  - Extended S-Band (2200 to 2450 MHz)
- IF bandwidths: Four (4), 0.5, 1.5, 5.0, 20MHz
- Tuner resolution: 20kHz
- Frequency accuracy: 0.005%
- Noise figure: Better than 6 dB
- Input level: -10dBm to –95dBm
- Damage free level: +10dBm
- 1st IF frequency: 280MHz
- 2nd IF frequency: 70MHz
- Processes PCM/FM NRZ codes - programmable from 50 kbps to 10Mbps NRZ codes, and 25kbps to 5 Mbps Bi-phase codes
- Codes can be NRZ-L/M/S, RNRZ-L (fwd/rev) or Bi-phase L/M/S per IRIG STD 106, programmable

BIT SYNCHRONIZER

Input Data

- PCM input: Single ended analog, programmable: 50 ohm, 75 ohm or 10K ohm
- Input codes: NRZ-L/M/S, RNRZ-L (fwd/rev) or BiØ-L/M/S per IRIG STD 106, programmable
- Analog input level: 0.1 to 5Vp-p
- Analog DC offset: Up to ±10V
- Bit rate:
  - NRZ Codes - Programmable from 80 Kbps to 10 Mbps
  - BiØ Codes - Programmable from 40 Kbps to 5 Mbps
- Accepts all IRIG-106 PCM inputs
- Provides all IRIG-106 PCM outputs with coherent clock
- Onboard bit error rate detector and test data simulator

Performance

- Loop bandwidth: 0.05% to 0.7% of bit rate, programmable.
- BER measurement: Measures errors on a PRN(n=15) pseudo random pattern. Up to 255 errors counted over (up to) 255M clock periods per measurement

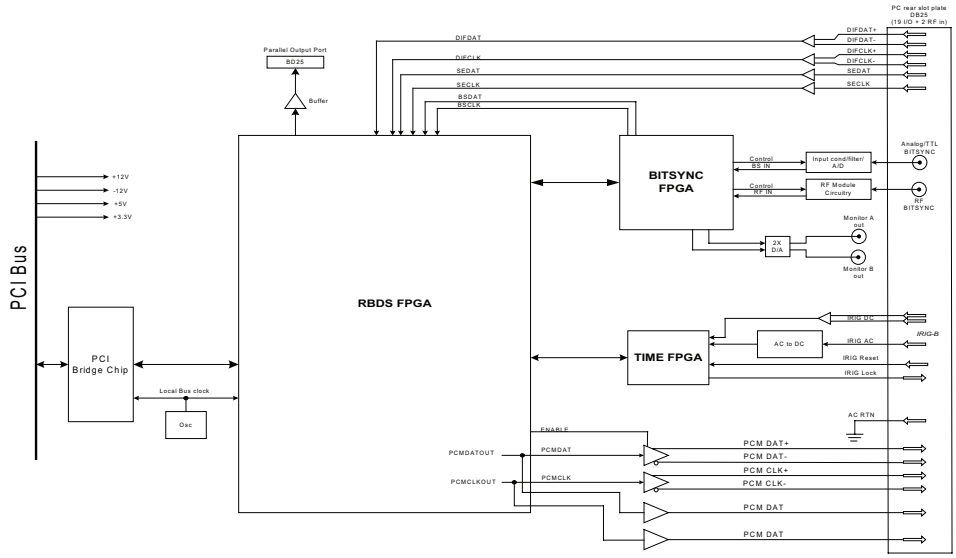
DATA DECOMMUTATOR

Input Data

- Inputs: NRZ-L data and clock. RS-422 (120 ohm) or TTL (10K ohm)
- Polarity: Programmable for normal (0 degrees), or inverted (180 degrees)
- Rate: Up to 20 Mbps (RS-422) or 10 Mbps (TTL)
- Time source: IRIG AC, DC or Free-Run from Time circuitry
- Sync pattern: Up to 32 bits programmable
- Sync mask: Any bit/s mask, programmable
- Lock strategy: Programmable for 1 to 16 good frames to acquire LOCK
- Drop lock: Programmable for 1 to 16 bad frames to drop LOCK
- Bit slip: 0, ±1, ±2, ±3 bits programmable
- Bits per word: 8 to 16 programmable
- Time: Microsecond of the year for each Minor frame
- Minor frame length: Up to 1024 words per minor frame
- Major frame length: Up to 256 minor frames per major frame
- Major frame: Major frames are handled by PC application
- Major frame sync: SFID and sync bits
- SFID: Programmable at any word
- Onboard minor frame time tag
- Word select mode: Any or all words from the format can be steered to this PCM output

SIMULATOR

- PCI bus: Interface for setup/control/status/power
- Status indicator: TTL compatible. Bit Sync Lock, Frame Sync Lock, IRIG Lock
- PCM output port: Programmable bit rate up to 20Mbps, TTL and RS-422 and has four (4) output modes:
- Playback: Playback of stored files
- Loopback: Internal TTL bit sync output directly feeds PCM output
- Word Select: Any or all words from decom can be steered to PCM output
- Random number generator for checking bIT sync integrity
- Parallel output port: Provides 16 bit frame word data and all control signals necessary to cherry pick any or all words from frame.



RBDS-120 block diagram

IRIG-B Time Code Reader

- Input format: Accepts IRIG-B in either AC or DC forms
- IRIG-B AC in: 0.5V to 10V p-p with nominal ratio of 3:1
- IRIG-B DC in: TTL differential per RS-422
- Acquisition/tracking: Automatically synchronizes to an externally applied input. Will “Flywheel” upon removal of input
- Time lock output: Provides TTL level Lock signal indicating “LOCK” to the selected time source (IRIG-B AC or DC)

Specifications

Status Indicators (over Bus)

- Bit slip indicator bit
- Flywheel indicator bit
- Decom in check state
- Decom in search state
- Clock present indicator
- Data present indicator
- Minor frame lock indicator
- Major frame lock (by software application)

General

- Supply current: +5V @ 700mA, +3.3V @ 650ma, +12V @ 400ma, -12V @ 0ma
- Power consumption: 11W maximum
- Operating temperature: 0 to 45°C (box ambient temp)
- Storage temperature: -20 to 85°C

Dimensions and Mechanical

- Weight: 20 oz (570 grams)
- Connectors: Standard PC, PCI connector and SMA RF connectors
- PCI card: Standard full size PCI card conforming to PCI spec r2.2

Ordering Information

Contact Curtiss-Wright for ordering information