

Multi-channel, Multi-board Coherency for SWaP-Constrained SIGINT and EW

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Introduction

Many new SIGINT and EW systems are being deployed on small platforms but still require sophisticated capabilities, such as multi-channel, multi-board coherency that enables beamforming. This white paper will discuss an effective approach to meeting these requirements with powerful FPGA technology build on the 3U OpenVPX form factor.

SIGINT Beamforming Requires Multi-channel Coherency

For SIGINT and EW systems, such as RADAR Warning Receivers, knowing which direction the signal of interest is coming from is as important as knowing about the signal itself. After all, if you have hostile ground-based targeting RADAR taking an interest in your aircraft, knowing where and what could be a matter of life and death. Beamforming is a signal processing technique that enables direction finding by using an array of antenna.

Beamforming works on the principal that differences in Time of Arrival for a signal at each antenna are proportional to differences in path distance from the source. By adjusting the gain and phase in each path, the antenna is electronically 'steered' (without physical movement) to locate the arrival angle of a signal; two or more arrays are used to triangulate the location of the signal source. The algorithms to accomplish this are highly compute intensive but lend themselves to parallelization.

For all this to work, the input channels from each antenna must be coherent, which requires precise clock timing and synchronization. In deployed systems the antenna will be at different points on a platform; for example, the wing tips, nose and tail of an aircraft. To maintain coherence across the input from these antenna, all the sensor inputs must be precisely aligned and the captured data calibrated and time-stamped. This starts at the analog inputs but flows all the way into the digitized data pipeline, because if the sampling instance is not aligned, there is a greater uncertainty of the signal interest's true bearing. And, for all but the smallest systems, this multi-channel synchronization must be extended across multiple analog inputs on multiple boards that are processing the analog inputs.

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Radar Warning Receiver Example

Radar Warning Receivers (RWR) use a number of RF inputs, typically between four and six channels. These are at fixed points around the aircraft; the associated data paths are calibrated and RF fed into each of the ADCs. The relative delay of the wave front across the antennas (and ADCs) can be directly correlated to the direction of that emitter, such as a targeting RADAR. This means that the accuracy of the synchronization between all the ADCs, even if they are spread across multiple cards, defines the baseline accuracy of being able to distinguish direction. Just one sample cycle error results in a very large error in the certainty of direction.

The example system below shows three VPX3-530 quad receivers, controlled by a single SBC, all three cards hooked up to a stopped common clock. The combination of the master clocking, and the ability to stop for multi-card sync, enable precise synchronization to be established. The backplane data paths allow the data to be streamed to a common FPGA and therefore to be processed to create the Pulse Descriptor Words (PDWs). The amount of processing required and the real-estate required to fit the require converters means that (today) it's difficult to fit it on a single small factor card, making multi-board sync a key consideration.

New SIGINT and EW Systems Have Additional Demands

Today's SIGINT and EW systems face additional, growing challenges in two dimensions. First, they must operate at higher and higher frequencies, as adversaries seek to avoid detection by moving their communications into the L-band. Coherence at higher frequencies demands extremely precise clocking and very low latency processing of the signals. The requirement for lower latencies is putting a premium on high performance parallelization of beamforming algorithms. And, in addition to parallelization, there must be low latency methods for merging the multi-channel data flows so that they are aligned on the correct data sample.

The other dimension of challenge is driven by a growing need for SIGINT and EW in positions closer to the warfighter. Capabilities that were initially deployed on a few large platforms, and used by theater-level operations, are now required in some form or other across the battlefield. This means that sophisticated systems are now being deployed on a range of smaller platforms, with all the resulting SWaP constraints.

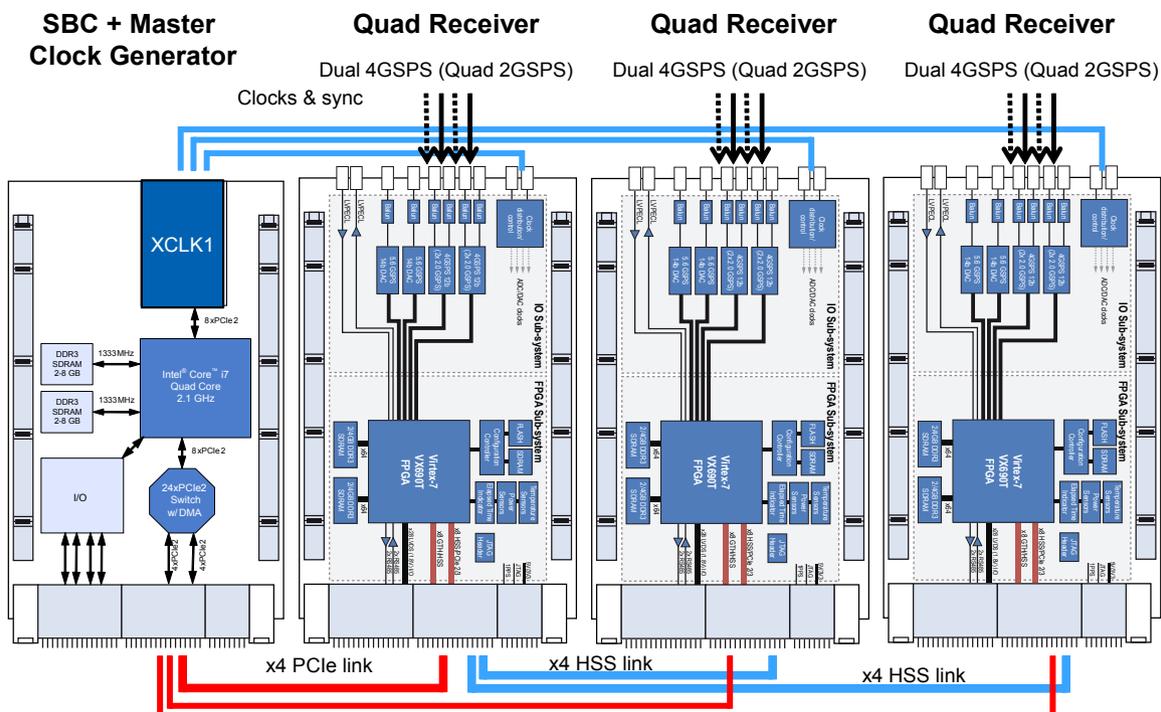


Figure 1: Example of a Radar Early Warning Configuration

Technology Trends – Powerful FPGAs & 3U OpenVPX

To meet the SIGINT and EW performance challenges, especially those for low latency processing, system designers have adopted FPGAs. For high speed digitization, the use of devices like FPGAs is usually the only practical way to catch and process the data. After an ADC digitizes a signal, it moves to an FPGA that acts on it; for beamforming this includes digital down conversion and filtering, then gain and phase adjustments.

Because they can implement extreme parallelism, with hundreds of DSP blocks operating in parallel, FPGAs are very well suited for processing intensive beamforming operations. As new generations of FPGAs evolve, they deliver more performance and greater I/O capability, allowing new designs to keep pace with more stringent requirements. For example, the Xilinx® Virtex®-7 FPGA delivers roughly twice as much processing power as the previous generation Virtex-6.

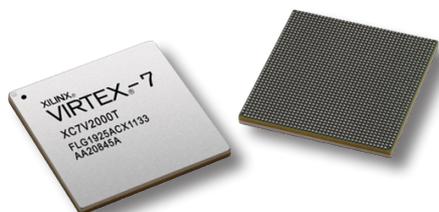


Figure 2: Xilinx Virtex-7 FPGA,
twice the performance of the Virtex-6

An FPGA implementation also permits optimization by IP that insures coherency across multi-channel data flows. This type of IP, specific to beamforming, executes low-level FPGA operations with great efficiency.

Addressing the SWaP constraints of small platform SIGINT and EW demands a small form factor solution. A wide range of embedded defense applications are moving to 3U OpenVPX™ as an effective, flexible industry standard. The compact size and modularity of the 3U form factor makes it a popular choice for the latest defense applications, while the OpenVPX standard is designed to directly connect cards with high-speed serial fabric on the backplane

Taken together, these two tech trends point to the need for solutions implementing the latest generation of FPGAs on a 3U OpenVPX module.

The VPX3-530 3U OpenVPX Virtex-7 FPGA ADC/DAC

The Curtiss-Wright VPX3-530 is a current example of a board designed to meet SIGINT and EW requirements for low latency beamforming operations with multi-channel, multi-board coherency. The VPX3-530 is a rugged dual channel 4 GSPS ADC/DAC packaged in the compact 3U OpenVPX form factor. The card has a user-programmable Xilinx Virtex-7 FPGA linked to two 4 GSPS 12-bit (or four 2 GSPS) analog inputs and two 5.6 GSPS update rate (maximum 2.8 GSPS data rate) 14-bit analog outputs with XC7V690T FPGA.

The VPX3-530 provides in one unit all the necessary I/O resources for the ADC, DACs, high-speed DDR3 SDRAM, high-speed PCI Express® (PCIe) and serial links – along with FPGA-driven parallel I/O to the OpenVPX backplane. At the core of the VPX3-530, the user-programmable Xilinx Virtex-7 VX690T FPGA is supported by high-speed DDR3L memory resources. These include flash memory or DDR SDRAM configuration memory, which are capable of storing FPGA configuration images. The host CPU, by way of a PCIe interface, updates these images. Configurations are downloadable from the host, through DDR SDRAM, bypassing the non-volatile flash.

At higher frequencies, multi-channel, multi-board synchronization can be challenging. There are layers of synchronization that come into play starting with the clock source. For multi-channel synchronization a master clock reference is essential for coherent operation. It must also be a good quality clock because jitter directly translates into noise – and at higher frequencies, the jitter becomes more significant. Supporting VPX3-530 is the XCLK1, a multi-channel, high quality, low jitter, phase matched output clock generator. The XCLK1 can use either an onboard clock source or an even higher quality external reference to drive the XCLK1 fanout buffers.

When preparing for multi-channel, multi-board synchronization using the XCLK1, the VPX3-530s in a configuration will undergo a synchronization phase via a user application command. This primes each of the VPX3-530 via a trigger in and out daisy chain to enter this mode. During this cycle, the XCLK1 is momentarily held in reset (the sample clock is stopped). This allows the ADC data paths

to be aligned in various ways. For example, each ADC has a demultiplexed digital interface and so the correct sample in the pipeline needs to be matched up to the correct sample clock (and dividers). Once complete, the XCLK1 clock outputs are released in a controlled manner (no glitches) ensuring that the ADC will be allowed to digitize data and that all ADCs are released at the same time. Further IP monitors the ADCs to ensure the devices remain in sync and in particular over temperature.

The timing parameters needed to achieve cycle-accurate, coherent sampling at these speeds, up to 4 GSPS, accounts for the majority of the IP that comes supplied with the VPX3-530.

Summary

Direction finding applications require beamforming with coherency across channels from an array of antenna. At high frequencies, this requires an ADC card with powerful FPGA processing, precise clocking and IP supporting low latency synchronization.

The Curtiss-Wright VPX3-530 meets these requirements within a compact 3U OpenVPX form factor, enabling highly effective SIGINT and EW implementations on small platforms.

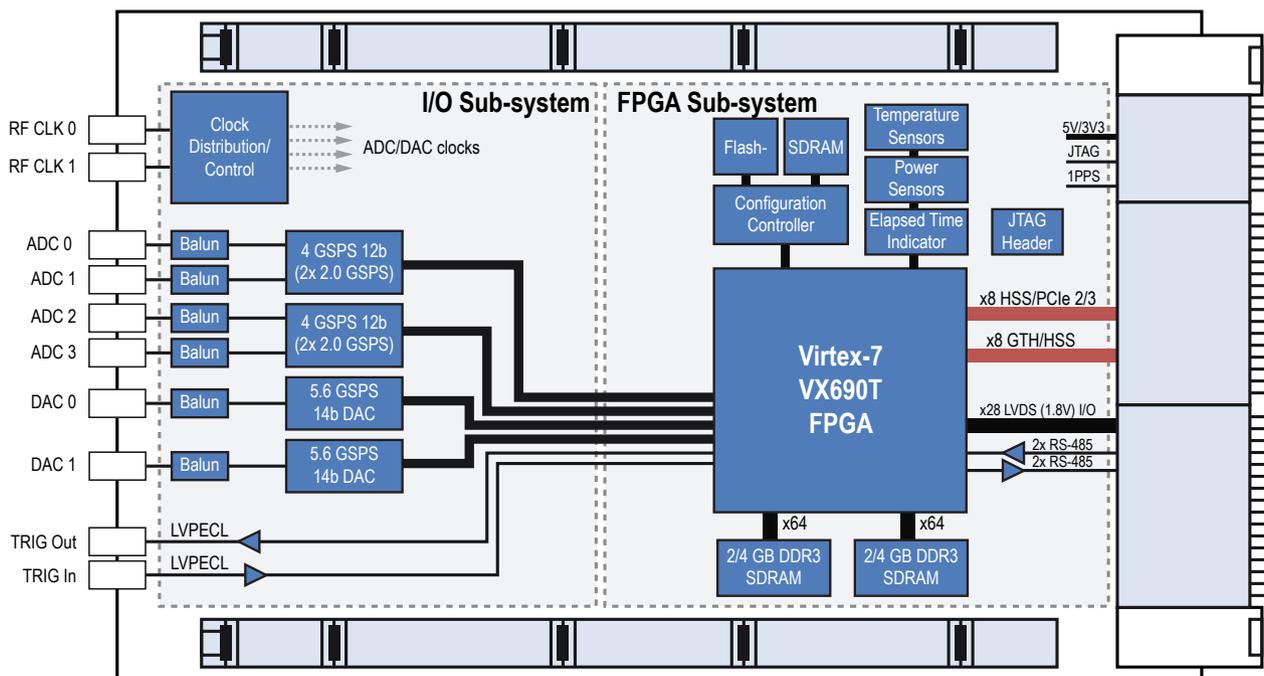


Figure 3: Figure : VPX3-530 Block Diagram

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[VPX3-530 Dual 4 GSPS ADC](#)