Introduction

Since its introduction in 2003, the VPX (VITA 46) standard has superseded the earlier VMEbus as the de facto board format for building rugged commercial-off-the-shelf (COTS) embedded aerospace and defense systems. Like most good open architecture specifications, VPX has evolved with the support of related complementary specifications standards that expand its ability to solve particular issues, such as new IO standards, better cooling methods, environmental enhancements and even test regimes. This ability to evolve and keep pace while new technologies and application requirements emerge helps to keep VPX relevant and maintain its stature as the form factor of choice for contemporary aerospace and defense applications.

Because the introduction of new complementary specifications standards is an ongoing and continual process, it is useful for the system integrator to have an overview of the contemporary VPX landscape. This white paper provides a concise primer on the current VPX ecosystem and how its various specifications can work together to architect a wide range of rugged high performance systems.

The numerous specifications standards that comprise the VPX ecosystem, most developed and defined under the auspices of the VITA ([www.vita.com](http://www.vita.com)) trade association's VSO standards body, are logically architected to solve a wide range of practical issues to enable the design of high performance aerospace and defense systems, including:

- High speed serial IO backplanes
- Backplane compatibility
- Cooling
- Fiber-optic connectivity
- RF analog IO connectivity
- Extended environmental qualification

The following diagram provides an at-a-glance view of the VPX toolbox. This paper will help a system integrator identify which standard solves which issue and why it is important.
ANSI/VITA 46.0
The VPX Baseline Standard

The ANSI/VITA 46.0 is the primary VPX specification standard and was designed with aerospace and defense applications in mind. Like other successful formats, such as the VMEbus, VPX traces its legacy back to the IEEE 1101.1 and 1101.2 mechanical format standards, and leverages the specification’s definitions of the 3U and 6U card form factors. VPX addresses the need for high channel density, high-speed serial interfaces (multi-Gbaud) to a backplane such as PCI Express® (PCIe), Serial RapidIO® (SRIO) and InfiniBand® – along with user IO. Like the VME and VXS formats, VPX also provides sub-specifications standards that define how mezzanine IO, typically XMC (VITA 42) and/or PMC (IEEE 1836.1), is mapped to backplane connectors.

While the earlier VME standard defined a single interface (along with uncommitted user IO), the ANSI/VITA 46.0 standard offers flexibility in regard to which protocol can be used, the number of IO channels, and many other variables. OpenVPX also adds the concept of data planes, control planes, and user IO planes to better aid in the integration of system level solutions.

Shortly after VPX was first introduced it became apparent that each module manufacturer was implementing different IO patterns. This left it up to the system integrator to solve the problem of which VPX cards could work together and whether “standard” backplanes could be used in their implementation. In order to ease the integration and interoperability challenge, the VSO developed and defined the OpenVPX™ (VITA 65) standard as a follow-on specification to VPX.

The baseline specifications standards that define ANSI/VITA 46.0 VPX, and the associated “dot specifications standards” are listed below.

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>TITLE</th>
<th>STATUS (AT TIME OF REVISION)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VITA 46.0</td>
<td>VPX Base Standard</td>
<td>ANSI approved</td>
</tr>
<tr>
<td>VITA 46.1</td>
<td>VMEbus Signal Mapping on VPX</td>
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<tr>
<td>VITA 46.3</td>
<td>Serial RapidIO on VPX Fabric Connector</td>
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</tr>
<tr>
<td>VITA 46.4</td>
<td>PCIe Express on VPX Fabric Connector</td>
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<td>VITA 46.6</td>
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<tr>
<td>VITA 46.7</td>
<td>Ethernet on VPX Fabric Connector</td>
<td>ANSI approved</td>
</tr>
<tr>
<td>VITA 46.8</td>
<td>InfiniBand on VPX Fabric Connector</td>
<td>(Trial Use)</td>
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<td>VITA 46.9</td>
<td>PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules</td>
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<td>VITA 46.20</td>
<td>VPX Switch Slot Definition</td>
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<td>VITA 46.21</td>
<td>Distributed Switching on VPX</td>
<td>Moved to VITA 65</td>
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Figure 2: Typical VPX card
**VITA 65**

The OpenVPX System Specification

VITA 65, usually referred to as OpenVPX, codifies a VITA/ANSI 46 VPX card’s backplane IO and system architecture and defines other interconnects like the data plane pipes. For example, VITA 65 defines the width of data plane pipes, (i.e., a “fat pipe” is x4 differential pairs), how many there are, where in the backplane they are located, and what protocols they support, etc. VITA 65 defines data plane pipes for both host and peripheral cards. Since the position of this connectivity is also defined, the specification enables the OpenVPX profile of a specific card to be examined to determine whether it is compatible with other cards in the system from a hardware and protocol point-of-view.

Over the last 15 years, vendors have developed a vast number of VPX cards. Accordingly, there are many profiles formally defined within OpenVPX. Periodically, additional profiles are added – usually to reflect newer protocols, such as newer generations of PCIe.

The list of profiles has now been split out in a dot specification standard, available as an Excel spreadsheet, to more conveniently list the various types. An OpenVPX slot profile, a key feature of the specification, is defined by the structure in the diagram below:

![Figure 3: Generic OpenVPX slot profile](image)

One example of an OpenVPX slot profile might be SLT3-PAY-2F4F2U-14.2.11. In this case the profile names denotes a 3U slot payload card with two data plane fat pipes, four expansion plane fat pipes and two control plane ultra-thin pipes on defined backplane connections. This paper is not intended to provide decoder details, but rather to help explain the information that OpenVPX specifications standards convey. There are also similar profiles for backplane and modules. For more details, refer to the ANSI/VITA 65 OpenVPX specification standards.

- ANSI/VITA 65.0; OpenVPX: System Standard
- ANSI/VITA 65.1; OpenVPX: System Standard Profile Tables

**VITA 66**

Blind Mate Backplane Fiber-Optics

The use of fiber optics can both solve and create a number of system design problems, particularly for rugged applications. Typically, fiber-optic connectors are relatively bulky and the associated cables have significant bend radii. For example, a popular LC connector type, with full duplex cables, might require ~25 mm of front panel real estate, with a cable bend radius of ~50mm. For a rugged system, these physical requirements can make system integration difficult, assuming there is even available space. In comparison, fiber-optic ribbon cables offer better bend radius, and are supported by two of the VITA 66 dot specifications. Additional dot specifications define the use of expanded beam and ARINC 801 footprints. See Figure 2 for a blind mate comparison.

VITA 66 replaces one, or more, of the VPX wafer blocks with a blind mate adaptor. The net effect of having backplane fiber-optic IO is to improve system maintainability that releases a valuable front panel area and mitigates fiber-optic cables from being damaged. Using a blind mate adaptor to mate a fiber-optic port to a fiber-optic connector via the backplane frees the fiber-optic transceiver from needing to reside on the host. This means that the transceiver could also reside on a mezzanine card on the VPX/VITA 66 host. Newer fiber-optic transceivers often replace the VITA 66 blind mate connector directly. This can provide some space savings, because even the latest generation of transceivers is bulky.

Today, the system integrator has a wide range of fiber-optic transceivers, offering good channel density and 10s Gbaud per fiber data rates from which to choose. This makes the options for using rugged fiber-optic interfaces better than ever, and the VITA 66 sub-specification standard makes them easier to design into VPX systems.

**VITA 66 standards:**

- ANSI/VITA 66.0-2016: base standard
- ANSI/VITA 66.1-2012: MT variant with each ferrule allowing up to 24 fibers
- ANSI/VITA 66.2-2013: ARINC 801 variant allowing up to 4 fibers
- ANSI/VITA 66.3-2012: Mini-Expanded Beam variant with up to 4 fibers
- ANSI/VITA 66.4-2016: Half size MT variant with MT ferrule supporting up to 24 fibers. This variant is particularly useful for 3U VPX which would otherwise give up half of its IO backplane IO connectors.
**VITA 67**

**Coax IO to Backplane**

VITA 67 solves similar issues to ANSI/VITA 66, but addresses the use of coaxial cables instead of fiber-optics. The use of coax cables is typically used to support RF IO and clocks that go beyond the capabilities of a standard VPX backplane connector. Since RF coax cables are even bulkier than fiber-optic cables, a backplane (blind mate) scheme offers significant advantages for system integration. This is especially true in applications that require a rack of high-density analog IO cards, because of the difficulty of removing the cards without removing all the cabling. Inserting and removing RF coaxial cables can be laborious due to the chores of routing the cables correctly and “torqueing” all the connectors. What’s more, conduction-cooled systems typically prefer little or no front panel connectivity. This is to reduce cabling issues and to maximize ruggedization and thermal performance, since “front panel” heat frames are an important heat flow component.

**VITA 66 standards:**

- **ANSI/VITA 67.0:** Coaxial Interconnect on VPX (base standard).
- **ANSI/VITA 67.1:** VPX, 3U, 4 Position SMPM Configuration. The blind mate fits into half of a VPX connector space.
- **ANSI/VITA 67.2:** VPX, 8 Position SMPM Configuration. This blind mate take a full VPX connector space.
- **VITA 67.3:** Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane (draft). This exploits 1” pitch to increase the number of connections possible with some flexibility of the connector type. Sub variants support both half and full VPX connector widths.

**VITA 48**

**Enhanced Cooling**

VITA 48 goes by the formal description, “Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)”. This group of standards defines schemes for enhanced cooling beyond conventional air and conduction cooling. See further down for information on different “dot” standard falling under VITA 48.

ANSI/VITA 48 enables the design of VPX systems to handle much higher power dissipation when needed. In the aerospace defense community, ANSI/VITA 48 is more important than ever because of the increasing power demands and increasing heat density. Although newer devices like FPGAs are much more efficient because of the shrinking geometries, their increased gate count also means that the overall power could actually be higher from generation to generation. While this enables more functionality in a given space and a possible reduction in board count, while power is reduced, heat density could be increased.

For example, one of today's 3U VPX cards with a mid-to-large Xilinx® UltraScale+™ FPGA and the latest generation of ADC/DAC devices might dissipate 150-200W. That can be even more than the much larger 6U format is able to cool using conventional technology. Previously, the power dissipation of such a card, albeit with lower performance, might be closer to 100W. The issue is not just with large FPGA-based cards. Cards based on latest generation Intel® Xeon® D or GPGPUs with their huge amounts of processing capability still need to be cooled in +85°C card edge environments. While 3U cards >100W can be cooled, they may require more exotic heat frame material and carry a significant cost premium. VITA 48 offers more cooling options, using more conventional material to duct cooling air or liquid, provided liquid or forced air within the system is available. At the board level, VITA 48 cards are comparable in cost to conventional conduction-cooled designs.

ANSI/VITA 48 also supports 2 Level Maintenance (2LM) to address mechanical and ESD protection of board level products, which is of particularly importance for removing and replacing cards in the field.

Also, due to differing requirements for component size and net power, different board pitches (0.8”, 0.85” and 1”) are defined.
**VITA 48 dot specifications:**

- **ANSI/VITA 48.0:** Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI) – Base specification
- **ANSI/VITA 48.1:** Mechanical Specifications for Microcomputers Using REDI, Air Cooling, Applied to VITA 46
- **ANSI/VITA 48.2:** Mechanical Specifications for Microcomputers Using REDI, Conduction Cooling, Applied to VITA 46
- **VITA 48.3 (Draft-inactive):** Mechanical Specifications for Microcomputers Using REDI, Liquid Cooling, Inboard QDs, Manifold Below the Backplane, Applied to VITA 46
- **VITA 48.4 (Draft):** Mechanical Specifications for Microcomputers Using REDI, Liquid Cooling, Inboard QDs, Manifold Above the Backplane, Applied to VITA 46
- **ANSI/VITA 48.5:** Mechanical Specifications for Microcomputers Using REDI, Air Flow Thru Cooling, Applied to VITA 46
- **VITA 48.6 (Draft-inactive):** Mechanical Specifications for Microcomputers Using REDI, Liquid Cooling, Outboard QDs, Manifold Above the Backplane, Applied to VITA 46
- **ANSI/VITA 48.7:** Mechanical Standard for Electronic Plug-in units using Air Flow-By™ Cooling Technology
- **ANSI/VITA 48.8:** Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling

It should be noted that ANSI/VITA 48.1, 48.5 and 48.7 do use patented inventions and would require appropriate licenses.

**VITA 47**

**Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard**

The VPX community is concerned with far more than electrical and mechanical standards. The VITA 47 specification defines a rigorous test regime that enables vendors to demonstrate to their customers that their VPX product is designed to perform optimally while complying with specific environmental, manufacture, safety and quality criteria. VITA 47 testing/verification includes: cooling, vibration, shock, humidity, altitude, rapid decompression, fungal resistance, ESD (including 2LM), corrosion resistance, workmanship (soldering, conformal coating and PWB fabrication), interchangeability, status lights, fans (including noise), safety (including materials, flammability and toxicity) and quality assurance.

By formalizing this test regime in a standard, the VPX community ensures that test procedures and results are consistent and meaningful. For example, VITA 47 calls for 500 thermal cycles, including minimum dwell times, which means that performing just one of these tests can take several days. Due to cost, and perhaps a lack of infrastructure, required to complete the full test regime, some vendors may choose to only cite the VITA 47 nomenclature and temperature ranges, rather than full VITA 47 compliance. Also, since VITA 47 involves a lot of additional testing, those vendors who do undertake the full VITA 47 regime might not undertake all the tests on all their module designs. When VITA 47 is cited for a particular product, it is a good idea to request a test report from the COTS vendor. The report should show that the module has been extensively tested beyond simple functional performance. Typically, the full regime of VITA 47 testing is only provided by larger vendors, particularly those with in-house test facilities.

**Conclusion**

The VPX eco-system is very active, vital and continually evolving. It successfully and comprehensively addresses the wide range of IO, interoperability, and ruggedization options needed to meet the requirements of the aerospace and defense market. In addition to the elements of the VPX ecosystem discussed in this paper, there are many more specifications that may apply. These include specifications for mezzanine card-based IO, including IEEE 1386.1 (PMC), ANSI/VITA 42 (XMC) or FMC (ANSI/VITA 57).
Next generation VPX cards are likely to be defined using most, if not all, of the baseline standards discussed in this document. That makes it important to have a familiarity and understanding of the VPX ecosystem and how the specifications fit together. Consider, for example, a new generation high-speed transceiver card using a high FPGA. This type of card is likely to touch on a range of VPX specifications, with a particular focus on the high power, high temperature related requirements supported by ANSI/VITA 48, which until now have been relatively uncommon.

Requirements and technology are constantly changing. The VPX standard has proven, as a “living document,” that it is able to adapt and thrive in order to keep the system designer ahead of the curve.

For additional information on VPX please see the VPX/OpenVPX tutorial on VITA’s website (http://www.vita.com/Tutorials).

Learn More

- **VPX (VITA 46) Standard**
- **VPX-REDI (VITA 48) Standard Modules & Systems**
- **OpenVPX (VITA 65) Standard**
- **VITA 47**
- **Air-Flow-Through (AFT) Cooling**
- **Ruggedization of Embedded Computing Boards & Systems**
- **OpenVPX Tutorial**

Further Information

- **VITA 48.8 AFT 3U VPX 6Gsps Wideband Transceiver FPGA Card**