Intel Xeon Cores Power High Performance and Low SWaP Complex Sensor Solutions

Read About

Multi-core Processors

Sensor Signal Processing

Imaging System Control

Modern day processors for imaging, radar, and other sensors are complex systems each unique with diverse processing requirements per company, platform, sensor, and application. A common feature is that these systems require high bandwidth and high performance signal processing. Such is now readily available with advances in FPGA capabilities as well as their programmability, the incorporation of embedded graphical processors, the increasing number of cores with vector units, and the high bandwidth of PCI Express and multi-Gigabit Ethernet.

Another common feature is that as the flexibility and power of these sensor systems has appreciated, so has the complexity of their software control. It is not uncommon for the architecture of embedded imaging and other sensor systems to have a framework of multiple software executables for the interface, data, and control processing.

For example, a passive infrared system in previous times might include a single monolithic imager which provided video from whatever was in front of where it was mounted. This simple technology-limited system didn't require much sensor, line of sight (LOS), targeting, or display functionality to control the hardware or process the target information from past signal processing capabilities.

This white paper will discuss how modern day processors can address the challenges of controlling today's more complex sensor systems using an IR imaging system example.

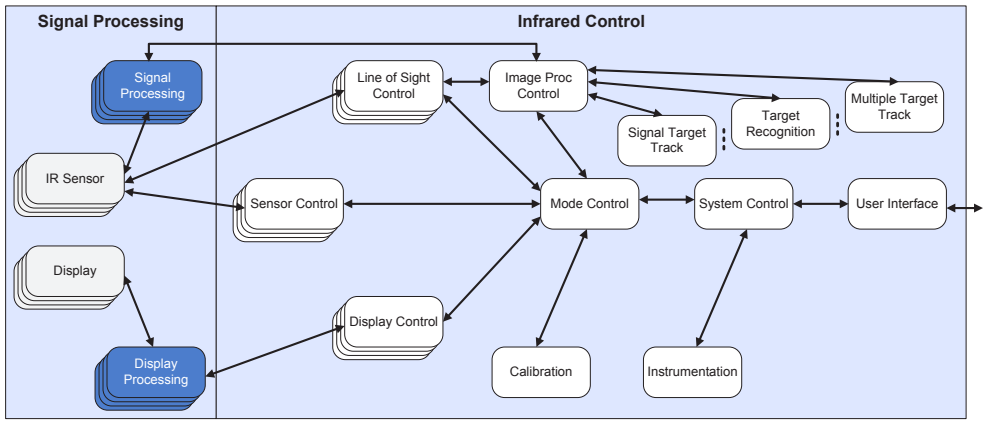

Figure 1: Image Sensor Control Processes

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Modern Imaging Sensor System

Today and tomorrow's imaging sensor system might include multiple sensor arrays each steerable and requiring multiple processes to control, point, display, and perform the data processing for a variety of image processing applications such as detection, recognition, and single target track as well as tracking multiple targets in the operational area. Figure 1 presents a simplified diagram showing some of the typical software processes for a multi-sensor, multi-targeting infrared (IR) system. Included among the control processes are the user interface, system control, pointing and stabilization, sensor control, instrumentation, calibration, image display, mode control, single and multiple target track, etc. There might be a multiple instances of some of these targeting processes depending on the application.

Some of the processing on the control side in today's software-driven systems has increased with higher frame rates, reduced latencies, more complex algorithms, and additional functionality. Some of the control processing has not increased, but engineers are not inclined to combine these software processes to avoid system development complexity. High-speed interfaces, FPGA, graphic, and multi-core digital signal processors have advanced sensor signal processing capabilities. The question is what can be done for the control side of the sensor processing.

A Multi-core Solution

For today's sensor architectures the recommended method for control processing is to exploit the increasing number of cores available in devices such as Intel's new Xeon D processor. The Xeon D processor has up to 16 cores, each with its own SIMD AVX2 vector engine. So not only is this processor capable of performing advanced signal processing, it is also available to host a multitude of software control processes. Multiple software executables that once required their own module slot can now be hosted on a single core of the Intel Xeon. As the signal processing footprint reduces, the control processing footprint is doing likewise using the same technology breakthrough.

There are advantages to this multi-core approach. Software developers integrate only a single processing executable per core using C/C++ programmability with a familiar embedded operating system such as VxWorks. Communication and synchronization between processes is simpler and faster without the need for dealing with the complexity of interfaces across chips. Intelligent control can now build configurable processing solutions where cores can be dynamically reallocated in real-time to processing different sensor modes. Intel has provided clock frequency control for individual cores so power can be configured where performance is needed and reduced where not required.

Figure 2 shows an example architecture for a four-sensor infrared processing system with image and display processing. For this system a graphics GPU is used for the front-end infrared image processing, extracting targeting information from the input video stream. The graphics GPU receives the infrared input in either digital or analog format from a frame grabber, processes the input image, routes imagery with commanded symbology to a display, and outputs targeting information. Multiple Xeon processor D cores can provide the system, line of sight, and video control.

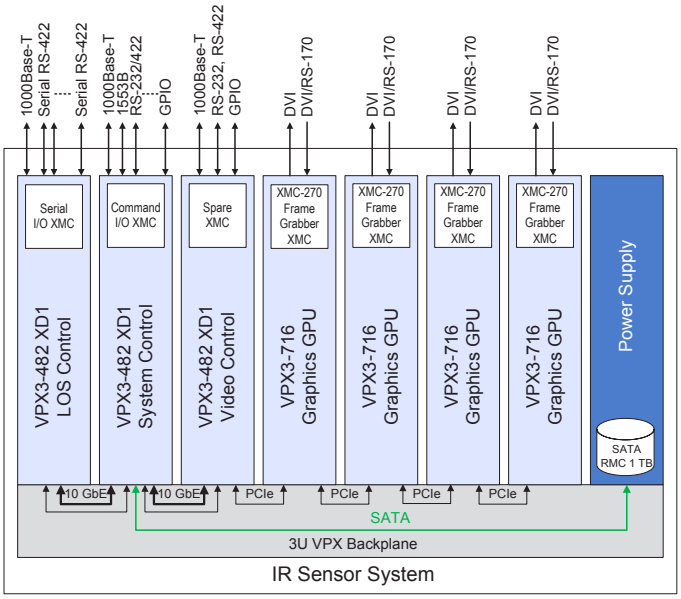

Figure 2: Infrared Sensor Processing Architecture

The CHAMP-XD1

Curtiss-Wright's CHAMP-XD1 utilizes this multi-core approach to better handle complex systems. Its video controller receives the target information and provides the back-end image processing and control. Its multiple cores can be allocated to host the different control and targeting software processes. For example one core might interface with the system controller while directing the rest of the image processing. Four of the cores might be statically assigned to direct the front-end image and display processing on the graphics GPU. Another core might be responsible for tracking of multiple targets across the full field of view. Because the target acquisition processing is situational and multi-functional, the remaining video controller cores might be dynamically allocated processing resources for a variety of targeting jobs such as track, recognition, etc. Each can extract video from the input streams and perform its commanded processing until tasked to do other processing. In one instance a targeting core might be switched from tracking one target to another or even tasked to perform another function such as recognition.

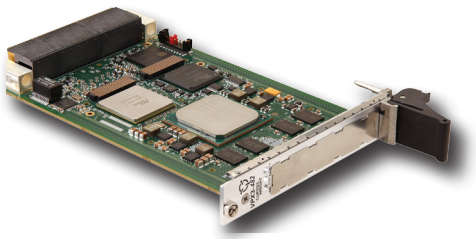

Figure 3: Curtiss-Wright CHAMP-XD1

The CHAMP-XD1 multiple cores also match well for sensor pointing and stabilization processing done on the LOS controller. Depending on the sensor configuration there are multiple control loops with feedback for each sensor platform. The loop rates are often variable for some of the sensor control hardware with feedback from the sensors and inputs from other systems such as navigation. For the four sensors in this configuration a line of sight control software process for each can be assigned to its own individual core. This process could provide that sensor's control, background, and lower rate loop processing. The remaining cores on the LOS controller could be allocated one or more of the high bandwidth control loops. Low latency communication interfaces from the LOS controller to the sensor hardware are provided through the available interface XMC on the CHAMP-XD1.

This still leaves a number of software processes for the third CHAMP-XD1, the system controller. Included among these are the user interface, mode, sensor calibration, instrumentation, system health, and other application specific control processes. This system controller's XMC can provide multiple additional command interfaces such as MIL-STD-1553B, ARINC 429, discretes, etc. For instrumentation a removable memory cartridge, mounted on the power supply with storage capability up to two terabytes, is interfaced over the system controller's SATA 3.0 interface. There is a PCIe Express x4 Gen3 backbone interface between system modules as well as a 10 Gigabit Ethernet interface between the system controller and the other two CHAMP DSP controllers.

Conclusions

The multi-core Xeon along with graphic and FPGA processors is a significant improvement for the sensor signal processing. It is definitely a game changer on the control side as well, both in terms of simplified software development and for reducing the SWaP footprint. In the multi-sensor infrared system example, the processing cores could be utilized for system, line of sight, and video control. The thirty plus cores allocated in the multi-sensor infrared processing architecture were supplied by only three Curtiss-Wright VPX3-482 CHAMP-XD1 DSPs.

These three CHAMP-XD1 DSPs, each with eight Xeon processor D cores with future versions to be available with 12 and 16 cores, provide what might have required up to ten quad-core processors of previous generations. The benefit is that a SWaP-optimal 3U OpenVPX architecture can now be configured as a multi-sensor image processing solution. An 8-slot 3U system (includes a spare slot) in the example configuration can be packaged in a 460 cubic inch (11.7 x 5.1 x 7.7") volume weighing less than 40 lb (18 kg) and dissipating under 600W. Leveraging the multiple cores now available for embedded systems with Intel's Xeon D processor, sensor processing solutions can be designed that allow customers to implement next generation embedded systems for imaging, radar, and other sensors in a small 3U OpenVPX format.

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