CASE STUDY

Advanced SIGINT Capability for a SWaP-constrained Platform

CURTISS-WRIGHT

DEFENSE SOLUTIONS

Challenge

- Detect and locate signals of interest very quickly
- Meet a small airborne platform's SWaP-constraints
- Coherent, low-latency processing for beamforming

Solution

- Four VPX3-530 3U FPGA ADC/DAC cards
- Two 4 GSPS 12-bit analog inputs on each card
- Xilinx Virtex-7 FPGA data stream processing

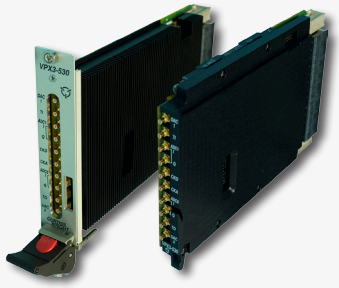
Results

- Rugged 8-channel SIGINT system
- Meeting latency and bandwidth requirements
- Deploying 3U OpenVPX COTS technology

Challenge

Curtiss-Wright recently engaged with a customer that was developing an airborne Signals Intelligence (SIGINT) system. The system needed to detect signals of interest at relatively high frequencies and determine the location of the signal source within a very small time interval. The airborne platform for the system was small, not a large wide-body aircraft.

The system designers needed an embedded computing system that could support signal acquisition from two sets of antennas and then process, with precision and low latency, the beamforming algorithms used for signal source location. For the location determination to work, the input channels from each set of four antennas had to be coherent, which requires precise clock timing and synchronization. The computing system also had to be rugged for airborne deployment and able to fit into the platform's size, weight and power (SWaP) constraints.



Rugged, air-cooled and conduction-cooled VPX3-530 cards

Solution

These challenging requirements were met by the Curtiss-Wright VPX3-530 3U FPGA ADC/DAC card. The VPX3-530 is a rugged dual-channel 4 GSPS ADC/DAC packaged in the compact 3U OpenVPX form factor. It has a user-programmable Xilinx® Virtex®-7 FPGA linked to two 4 GSPS 12-bit (or four 2 GSPS) analog inputs and two 5.6 GSPS update rate\ (maximum 2.8 GSPS data rate) 14-bit analog outputs with XC7V690T FPGA.

The VPX3-530 provides in one unit all the necessary I/O resources for the ADC/DACs - high-speed DDR3 SDRAM, high-speed PCI Express® (PCIe) and serial links – along with FPGA-driven parallel I/O to the OpenVPX™ backplane. For precise synchronization, the VPX3-530 is supported by the XCLK1, a multichannel, high quality, low jitter, phase matched output clock generator. The XCLK1 can use either an onboard clock source or an even higher quality external reference to drive the XCLK1 fanout buffers.

At the core of the VPX3-530, the user-programmable Xilinx Virtex-7 VX690T FPGA is supported by high-speed DDR3L memory resources. These include flash memory or DDR SDRAM configuration memory, which are capable of storing FPGA configuration images. After an ADC digitizes a signal, it moves to the FPGA that acts on it; for beamforming this includes digital down conversion and filtering, then gain and phase adjustments.

Additionally, the VPX3-530 is rugged, built to operate in harsh conditions, with air-cooled and conduction-cooled versions.

Results

In a rugged OpenVPX chassis, Curtiss-Wright's customer configured four VPX3-530s for an eight input channel system, along with an external clock generator and a 3U OpenVPX Single Board Computer serving as the system host and controller. This powerful but space-efficient system delivers what the application requires, a balance of low latency, FPGA processing to A/D channels, synchronization capability, sample rate, bandwidth and SWaP characteristics.

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