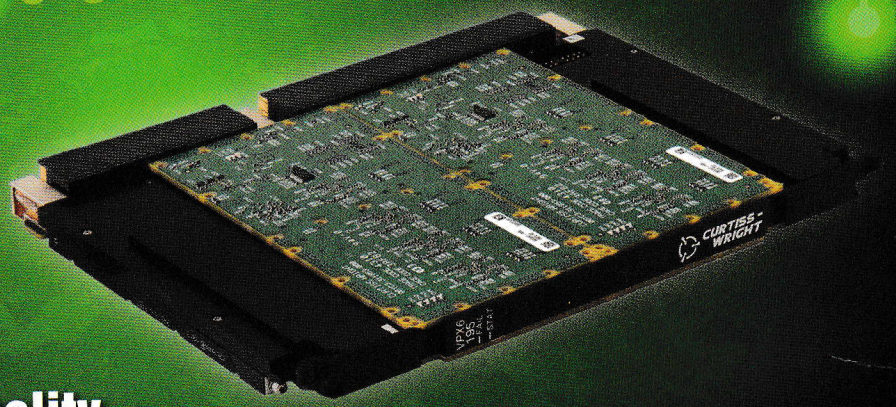

Product teardown: Maximizing functionality through dual-node processing

By Jerry Gipper

Aerospace and defense applications must support higher-bandwidth sensor input, more complex intersystem communications, and greater security for certain operations and related custom algorithms, all while contending with budget and schedule pressures. In addition to these broad challenges, application areas such as mission computing face the added difficulty of designing systems that meet restrictive size, weight, and power (SWaP) constraints. Increasing function density within a current space envelope is a common way of addressing these challenges.

Curtiss-Wright offers a VPX SBC – the VPX6-195 – that presents some interesting solutions to enabling today's complex applications. One major characteristic about the VPX6-195 that makes it stand out from other boards is its dual-node SBC architecture. The dual processing nodes are completely independent of each other, helping address SWaP constraints and performance challenges in ways that are not possible with a traditional single-node SBC. In essence, the VPX6-195 is two independent processor nodes in a single 6U slot package.

How is this done?

Curtiss-Wright designed the VPX6-195 right from the start to operate as two nodes. It has two Freescale T2080 quad-core 64-bit CPUs. Each processor has its own independent memory and I/O subsystems with backplane access. The VPX6-195 supports a rich I/O complement per processing node, which includes two GbE ports (one 1000BASE-BX and one 1000BASE-T), four serial channels, discrete and differential digital I/O, USB 2.0 ports, and an XMC site.

THE DUAL PROCESSING NODES ARE COMPLETELY INDEPENDENT OF EACH OTHER, HELPING ADDRESS SWAP CONSTRAINTS AND PERFORMANCE CHALLENGES IN WAYS THAT ARE NOT POSSIBLE WITH A TRADITIONAL SINGLE-NODE SBC.

Where the board starts to be distinctive is with the addition of a dedicated Xilinx Kintex FPGA and XMC slot to each node. The standard product comes equipped with a Kintex K70T FPGA, but can also be ordered with a larger Kintex K325T FPGA. The only common elements are system-level functions including intelligent platform management interface (IPMI), real-time clock (RTC), and temperature sensors.

The VPX6-195 provides four 10GBASE-BX4 ports for the VPX data plane fabric, two ports from each processing node to the VPX P1 connector. The processing nodes are also connected by two 10GBASE-KR ports for internode communication. For red/black (unencrypted/encrypted) applications, this can be disconnected.

Each processing node has a PCI Express (PCIe) connection to the expansion plane on the VPX P2 connector. Depending on the variant, the expansion plane connection can either be a four PCIe Gen2 port, two x4 Gen2 ports, or a single x8 PCIe Gen2 port.

To cost-effectively address a diverse range of military/aerospace applications, the VPX6-195 is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions available in Curtiss-Wright ruggedization Levels 0 and 100, and conduction-cooled versions in Levels 200 and 300 with line replacement module (LRM) covers.

Since each node on the VPX6-195 is independent of its mate, each can run a different operating system and applications. The card is supported by a suite of U-Boot, real-time operating system (RTOS) BSPs, communication libraries, and signal processing libraries. Throw on a hypervisor-enabled OS, and you can start to see some interesting ways to split the system.

Applications

SWaP-C optimization

The dual-node architecture means that two slots can be consolidated into one (see Figure 1). The impact on size is a reduction in card slots from two to one, with a possible reduction in mezzanine slots from four to two if the previous boards had mezzanine capability. Weight per slot is immediately reduced by 50 percent. Power dissipation is approximately the same, assuming the power on the SBCs being replaced is the same as a single node on the 195, but a higher performance/watt can be assumed. At the slot level, a VPX6-195 has power requirements as low as 80 W. System robustness has potential for improvement by reducing modules; however, it may remain nearly unchanged if the gained space is utilized. The cost impact is variable and dependent on the specific costs of boards that are being replaced and the utilization of the added capability of the FPGAs.

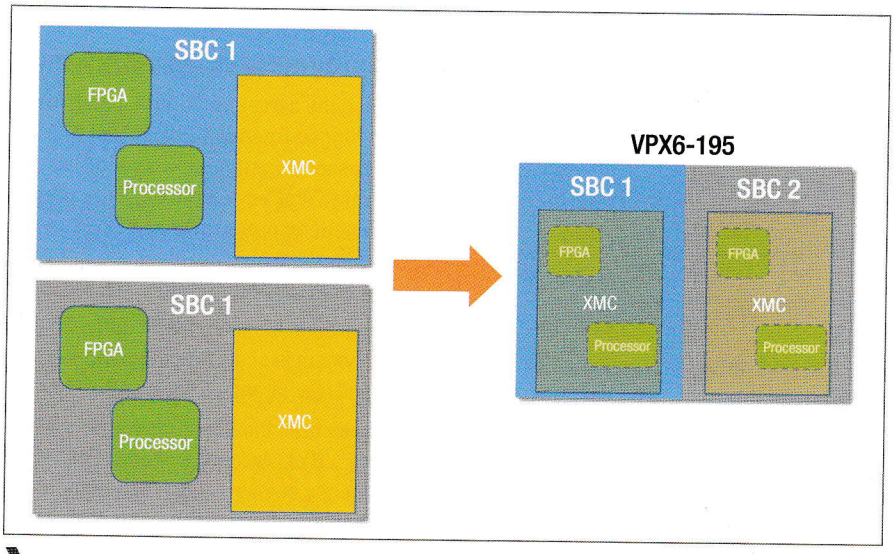

Figure 1 | Transformation from two slots to one slot

Red/black processing

Secure separation of red/black processing elements within a computing system is increasingly important for both commercial and defense system applications. Recent systems have taken advantage of hypervisor OS software to isolate systems, but with the VPX6-195, two truly independent hardware systems can also occupy the same VPX slot – the most secure and easiest to validate.

On the VPX6-195 any link between the two nodes can be disconnected by assembly population option, configuring the 195 as two independent SBCs on a single card. Curtiss-Wright has included other protections to ensure trusted computing and secure boot. Each node's FPGA has space for customer specific security functionality. The T2080 processor supports Freescale's Secure Boot architecture, with the ability to boot encrypted images so external key storage is not needed.

Mission computer applications

Many applications place the highest priority on processing performance. With the two Freescale T2080 quad-core 64-bit CPUs, the user gets the performance of the processors plus that of the Kintex FPGAs. Mission-specific IP can be loaded into the FPGAs to add functionality or offload application-specific processing.

ISR applications

Intelligence, surveillance, and reconnaissance (ISR) applications are specific cases that often need intense processing performance and complex I/O processing. The Xilinx Kintex FPGA comes in two sizes – the largest possible – to meet the most demanding ISR applications.

Advancements expand possibilities

Technology has evolved to enable configurations that were simply not possible a few years ago. Putting the functionality of a single processing node in a single 6U slot was a major challenge 10 years ago. Today you can put two on a single-slot 6U board and still have plenty of space for custom functionality in a large FPGA. Processor performance, FPGA density and performance, high-speed serialized I/O, and great strides in power utilization continue to make it possible to do the impossible.

Curtiss-Wright has posted a white paper titled "Enabling Complex Applications with a Dual Node Single Board Computer" with more details on using the VPX6-195 (see www.cwcdefense.com/products/single-board-computers/6u-ppc-sbc/vpx6-195.html). VT