CASE STUDY

Increasing Memory Capacity by 400% to Solve Sensor Fusion Challenges

CURTISS-WRIGHT

Challenge

- Customer has code that requires copious amounts of memory
- Customer only has access to 32 GB

Solution

- Curtiss-Wright's CHAMP-XD2M
- Achieve maximal potential with 128 GB

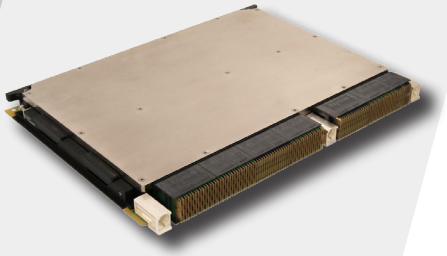
Results

- 400% increase in memory capacity
- Deploy code right out of the lab

Challenge

Today, modern sensors in all Intelligence, Surveillance, Reconnaissance (ISR) technology segments output more data than ever before. For instance, electro-optical infrared (EO/IR_focal plane arrays have far greater resolution and frame update rates than ever before. Radar phased arrays have higher element counts and higher I/Q bit depths on the egress. Signal Intelligence (SIGINT) systems have RF tuners with wider instantaneous bandwidths and therefore higher throughput digitized IF at the output. Additionally, all of these sensors have higher density channel counts than previous generation sensors.

A customer familiar with this problem came to Curtiss-Wright Defense Solutions with the added compound problem of Sensor Fusion applications; These applications often see a firehose of data from each of these ISR segment sensors that aggregate to a single processing subsystem. In some cases, even existing solutions such as the Curtiss-Wright CHAMP-XD2 6U OpenVPX™ modules with 32 GB of DDR4 per each of two Intel® Xeon® D processor devices become memory bound. Despite 32 GB representing an enormous amount of capacity, there is so much sensor data throughput at the ingress of a processing module in a Sensor Fusion application; even this amount of DDR4 is insufficient to buffer the onslaught of data.



CHAMP-XD2M

Solution

By removing one of the Xeon D devices on the existing CHAMP-XD2 dual Xeon D module, Curtiss-Wright's team of engineers was able to utilize the recovered surface area on both the front and backside of the VPX printed circuit board. This also meant the team was able to quadruple the memory capacity from 32 GB to the full amount of memory realizable off the Intel Xeon D processor: 128 GB. By unlocking this new level of memory capacity, the customer's sensor fusion challenges quickly dissolved.

The team also replaced the Xeon D processor SKU used on the CHAMP-XD2 with an alternate Xeon D SKU. This change increased the core count from eight to 16, and made up for the loss of the second node. This new product derivative driven by the customer's challenge is known as the CHAMP-XD2M (VPX6-483M).

Results

Tackling the challenge of only 32 GB of memory head on, the Curtiss-Wright team was able to offer the customer a 400% increase in memory capacity with a total of 128 GB. By increasing the capacity while keeping the Xeon D core count the same, Curtiss-Wright was able to provide the buffer depth needed by the Sensor Fusion application to allow a sufficient snapshot of aggregated sensor data to be prosecuted in real-time, with no loss of data. Of particular note, the CHAMP-XD2M's maximum memory topology represents state of the art in memory-down design, requiring the caliber of Curtiss-Wright's world-class engineering capability. This enables the production of a module that can meet the unparalleled demands of the ISR sensor-equipped warfighter.

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