CASE STUDY

Rugged CameraLink using Xilinx Kintex-7 FPGA

CURTISS-WRIGHT

DEFENSE SOLUTIONS

Challenge

- Implement CameraLink® interface to Xilinx® Kintex®-7 FPGA
- Provide a conduction-cooled solution

Solution

- XF07-523 LVDS I/O card
- CameraLink / ChannelLink™ emulation

Results

- Use of flexible I/O platform that already existed
- No need to develop hardware specific solution for CameraLink

Challenge

Traditionally, CameraLink solutions use specific chipsets designed to implement ChannelLink, the physical interface associated with CameraLink. ChannelLink provides a parallel interface that is then multiplexed a few serial lines – and then de-multiplexed at the other end of the link if required. CameraLink is often used for high-performance imaging, usually frame grabbers.

The challenge is to provide a direct CameraLink interface to a Kintex-7 FPGA without the need for ChannelLink transceivers, thereby allowing an existing “generic” digital FPGA solution to be used. This provides greater flexibility as the hardware is no longer CameraLink specific and can also be used for other digital I/O schemes, such as LVDS in the future.

The CameraLink interface needs to support the Full, Medium and Base I/O modes. Since the I/O is directly interfaced with a user programmable FPGA, data processing can be combined with I/O for a high performance imaging application.

Curtiss-Wright has previously supplied FPGA I/O cards with CameraLink/ChannelLink I/O modules along with CameraLink FPGA IP allowing customers to embed this IP into their FPGA based application – with a high speed DMA driven PCIe®/PCI-X interface for host interface and control.

XF07-523 FPGA Digital I/O XMC

Solution

The XF07-523 is a Kintex-7 based XMC available in both rugged air-cooled and conduction-cooled formats. The XF07-523 provides unbuffered, direct interfaces to an industrial grade K325T Kintex-7 FPGA along with local FPGA attached memories. The XF07-523 along with the FusionXF™ toolkit provides a user programmable FPGA resource as well as I/O interfaces for a combined I/O and high-performance data processing engine.

The XF07-523 has sufficient LVDS connections to support Base, Medium and Full ports – or a multiple of them through either the front panel (air-cooled only) and/or over XMC P16 I/O or PMC P14 IO. Base, Medium and Full ports require 11, 16 and 21 LVDS pairs respectively. For XMC P16 / PMC 14 based I/O over the host, one or two Base mode, one Medium mode or one Full mode can be supported. If the XF07-523 front panel I/O was also used (extra 32 LVDS pairs) then even more channels can be supported. In short, the XF07-523 offers the future flexibility of having more CameraLink ports with spare FPGA resource to embed a local application. Note: a suitable cable would be needed to connect to standard CameraLink devices. In addition, care needs to be taken as the CameraLink interface is unbuffered and directly connected to the FPGA. Therefore attention needs to be paid to cable lengths and the design needs to mitigate the possibility of voltage spikes, etc. – these can be effectively managed with good system design.

To allow this card to be used as a CameraLink I/O card, Curtiss-Wright has extended its IP to include de-multiplexing of the fast ChannelLink I/O using SelectMap parallel I/O pins of the FPGA, effectively emulating the functionality of the ChannelLink transceivers and layering its previous CameraLink IP on top. The specialist MGTs of the Kintex-7 FPGA are not required because of the speed of this generation of devices.

Results

Using a standard product like the XF07-523 offered the flexibility of using newer generation FPGAs to drive one or more CameraLink I/O ports in different modes. The result enabled a truly rugged conduction-cooled configuration without the cost of new hardware development.

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