CASE STUDY

The Bigger Picture for Radar Sub-systems

CURTISS-WRIGHT

Challenge

- COTS requirement, but customer specific additions
- Multi-discipline deliverables; hardware, software and HDL
- Fast development platform from first delivery

Solution

- High-speed VPX3-530 3U FPGA transceiver cards
- Flexible, semi-custom DDC IP cores
- Xilinx Virtex-7 FPGA data stream processing

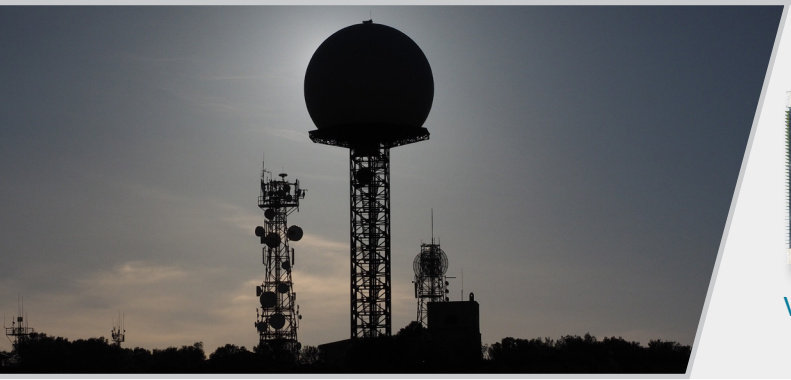
Results

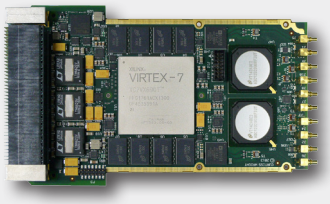
- Rugged, scalable 3U VPX sub-system
- Customer can focus on their core expertise from day one
- Clear point of contact for all aspects of sub-system

Challenge

A Curtiss-Wright Defense Solutions customer was starting to develop a new range of Radar systems. This involves solving a number of problems including: high-speed digitization with enough FPGA resource to develop their own application, semi-custom DDC IP that could be integrated with the customer's application, integration of other system functions such as SBCs and additional digitizers – all to be wrapped up in a rugged system. The customer had signal processing performance targets to match specific DDC characterization and SFDR performance criteria. High performance FPGA processing offers rich benefits, but can be challenging to tame especially if the multiple aspects of hardware, software, HDL and integration into a rugged solution come into play. The aim was to find a single vendor who could handle all of these factors, so the point of responsibility was clear.

The task was not to provide a Radar system, but rather a hardware platform ready for the customer to develop their application, focusing on their key expertise and value-add, knowing that all the interoperability and hardware integration aspects were in place – ready to hook up to their transmitters and receiver front ends.





VPX3-530: Multi-Gsps Transceiver

Solution

The key to this customer's challenge was working with a vendor who has a broad enough product line to provide all the pieces of the system, yet flexible enough to adapt standard products. Ultimately, all the advantages of COTS and the ability to get exactly what the customer needs rather than compromise.

The digitizer function was performed by the VPX3-530, a rugged dual-channel 2 or 4 GSPS transceiver packaged in the compact 3U OpenVPX™ form factor. It has a user-programmable Xilinx® Virtex®-7 FPGA linked to two 4 GSPS 12-bit (or four 2 GSPS) analog inputs and two 5.6 Gsps output rate (maximum 2.8 GSPS input update rate) 14-bit analog outputs. The VPX3-530 can directly digitize in the L-band or interface to tuners for wideband, higher frequency operation.

The VPX3-530 provided all the necessary I/O resources for the ADCs and DACs - high-speed DDR3 SDRAM, high-speed PCI Express® (PCIe) and serial links – along with FPGA-driven parallel I/O to the OpenVPX backplane. Future expansion is supported through the addition of multiple VPX3-530 cards, all controlled by a single SBC, and all fully synchronised. An XCLK1, master clock reference, can be conveniently sited on the SBC without requiring an additional system slot.

At the core of the VPX3-530 is a user-programmable Xilinx Virtex-7 VX690T FPGA supported by high-speed SDRAM memory resources for buffers and for moving data to the host SBC using high speed DMA.

Interfacing high-speed communication between FPGA cards and SBCs (or GPGPUs, DSP, etc.) can be challenging, especially if newer operating system support is required. Having a common vendor for elements of the system removed the risk of ongoing interoperability from the customer.

To leverage the hardware's capability, a wideband (decimate by 4) DDC IP core was provided, developed to be modular and adaptable. The DDC IP core was modified in line with the customer's DSP performance targets. Having the hardware vendor provide the IP core was the most efficient approach for the customer as the vendor has the most experience with, and deepest knowledge of the hardware, likely gained from other customization activities. This allowed the customer to focus on adding their IP to the data stream within the FPGA without needing to learn the architectural details. Whilst a semi-custom IP core, the core is still flexible and programmable including features such as decimation rates, filter coefficients, NCO phase adjustment and output format. By understanding the customer's requirements, the DDC IP core was also optimized for as small of a footprint as possible thereby maximizing the available FPGA resource for the customer application.

Additionally, the VPX3-530 is rugged, built to operate in harsh conditions, with air-cooled and conduction-cooled versions.

Results

Having a Curtiss-Wright Quick Start Kit (QSK) meant the customer was able to get up and running quickly, without the need to dig into low-level details in order to evaluate and start application development. The customer was able to focus on their own activities, while the vendor gave them the peace of mind they needed.

Like any complex development, additional support is inevitable. Curtiss-Wright's industry-leading customer support ensured the customer could be successful no matter any challenges that arose.

Following successful completion of the development phase and field trials, the customer's next phase is to implement a fully rugged system including the option of extending the number of digitization and FPGA resource for a scalable, deployable system secure in the knowledge that Curtiss-Wright's pedigree is in providing fully rugged, extensively tested solutions to the defense market.

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