CASE STUDY

Upgrade Airborne Radar within Power, Cost & Temp Constraints

CURTISS-WRIGHT

DEFENSE SOLUTIONS

Challenge

- Double the processing throughput of an existing airborne radar
- Upgrade the analog-to-digital converter (ADC) front-end
- Change I/O connectivity without changing PCB
- Stay within a strict power budget and under cost limits
- Operate reliably across a -40 to +85°C temperature range

Solution

- Start with a 6U OpenVPX board using three Virtex-7 FPGAs and two FMC sites
- Modify the BOM (Bill of Material), removing non-essential parts
- Use a pin compatible I/O Mapper to replace one FPGA and change I/O connectivity
- Integrate ADC FMCs with FPGA design

Results

- A rugged, high performance solution using the latest FPGAs
- Meeting all environment, power, performance and cost targets
- Upgrading radar capability across multiple airborne platforms
- A satisfied customer

Challenge

To remain competitive, a Curtiss-Wright Defense Solutions customer needed to upgrade an existing radar system deployed across multiple airborne platforms. A critical part of the upgrade was doubling the system's signal processing throughput; the customer's system engineers calculated a new generation of FPGAs could deliver the required performance. However, any design with new FPGAs also needed to supply them with input via flexible, high-bandwidth analog interfaces to the radar antennae and similarly high-bandwidth output to the rest of the system.

In addition to the throughput requirements, the system engineers also faced three stringent design constraints. First, the radar upgrade had a fixed cost target, driven by the competitive nature of the market; this cost target flowed down to all components, including the signal processing. Just as fixed was the power budget, driven not by competition but by limits in the power available in airborne platforms. And lastly, because the radar system would be deployed in the harshest environments, any signal processing modules had to be able to operate reliably across a -40 to +85°C temperature range.

Solution

Curtiss-Wright engineers engaged with the customer's design team to craft a solution. They started with the CHAMP-FX4 6U OpenVPX™ FPGA processing module; it has three large Xilinx® Virtex®-7 FPGAs with abundant memory and I/O interfaces, including two FMC sites. However the CHAMP-FX4 far exceeded the power and budget constraints of the program. Furthermore, due to the high power, the default configuration of the CHAMP-FX4 would not meet the top-end thermal constraints. Curtiss-Wright then began to modify the CHAMP-FX4 design, removing parts not essential to the radar upgrade and replacing one of the FPGAs with a smaller pin compatible FPGA.

A key part of this design customization was replacing one of the three Virtex-7 FPGAs with an I/O Mapper. This small printed circuit board (PCB) fits into the space previously occupied by the FPGA, with pin connections to the interfaces that had connected to the FPGA. Some of these interfaces are redirected to the backplane connector, providing more system I/O and other interfaces are reconnected, providing additional communication bandwidth between the two remaining FPGAs. This custom design was done in such a way as to not impact the I/O of the remaining FPGAs. The I/O Mapper enabled the new board to meet connectivity and backplane I/O requirements that would have otherwise required an expensive respin of the CHAMP-FX4 base PCB. Functionality of the I/O Mapper was validated to insure all requirements were met.

Further reductions in cost and power draw were achieved by removing a Serial RapidIO® (sRIO) switch and an sRIO to PCI Express® (PCIe) bridge, as well as unneeded memory chips. The overall design of the CHAMP-FX4 was not radically altered but simply modified to meet the radar upgrade needs.

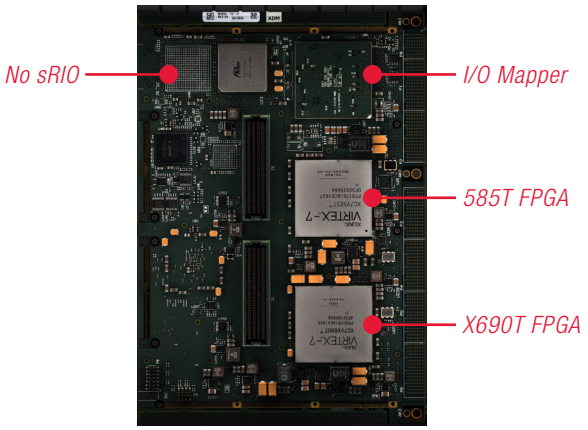
Along with the design modifications, there were certain application-focused configuration details. Specific Virtex-7 parts were selected because of their lower power requirements and Analog to Digital Converter FMCs were selected to meet antennae input specifications.

Result

This successful design demonstrated the strong collaboration between customer and supplier that Curtiss-Wright strives for. As technology continues to advance and design constraints become more difficult, it is important to have a partner that will work with you to find the most efficient path to the end goal.

The customized 6U OpenVPX CHAMP-FX4 has successfully passed full Level 200 qualification (-40 to +85°C) along with shock and vibration testing and successfully met customer's requirements. It provided the required processing throughput increase, while staying within power, cost and temperature constraints. Furthermore, VxWorks is running on the dual-ARM Cortex A9 processor within the Xilinx Zynq SOC FPGA that is located on the card, providing a power efficient single card solution. The radar upgrade program has passed several field trials and is moving into deployment on a few different programs.

For more information about the CHAMP-FX4, please refer to the CHAMP-FX4 product page on our website, our white paper Delivering Signal Integrity with High-performance FPGAs & Gen3 Bandwidths or view the on-line video CHAMP-FX4 6U OpenVPX FPGA Processing Module.



Curtiss-Wright's modified CHAMP-FX4

Platform images courtesy of Defenselmagery.mil

INFO: CURTISSWRIGHTDS.COM
EMAIL: DS@CURTISSWRIGHT.COM

© 2015-2017 Curtiss-Wright. All rights reserved. Specifications are subject to change without notice.
All trademarks are property of their respective owners | A21.0217