CASE STUDY

Meeting the Challenge of Direct Sampling of SATCOM Data

CURTISS-WRIGHT

DEFENSE SOLUTIONS

Challenge

- Process full S-band frequency range without down-conversion
- Reconfigurable platform requires large amount of FPGA processing
- 100-200 Gbps of interconnect bandwidth between FPGAs

Solution

- 6U OpenVPX™ FPGA card with 12 Gsps ADC/DAC module for the front-end
- 3 large Virtex-7 FPGAs
- Simplex RTM to enable TX and RX SerDes links to be daisy-chained to different devices

Results

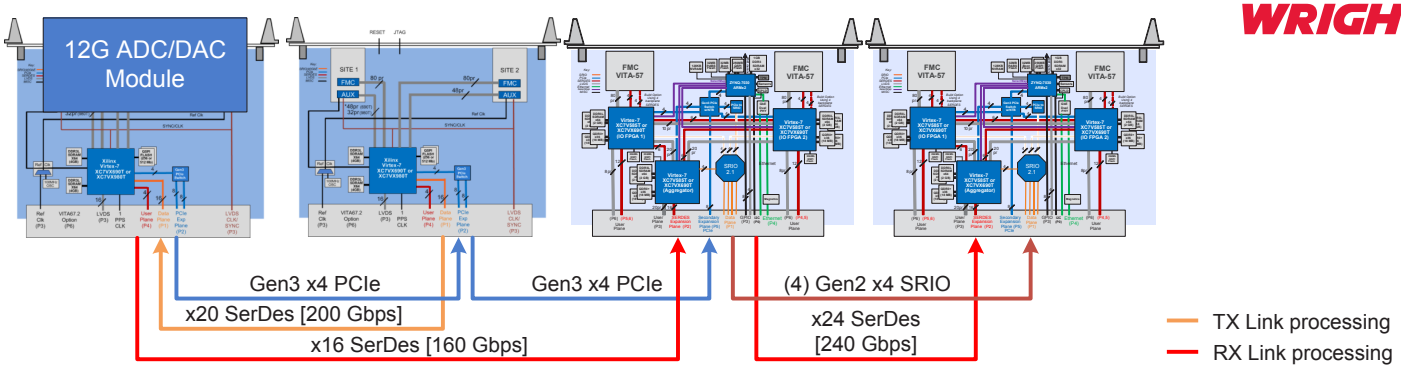
- A modular, scalable powerful SATCOM system
- Reconfigurable architecture that can be updated via firmware
- Meeting all performance requirements

Challenge

Many satellite communication (SATCOM) systems use S-band (2-4 GHz) and C-band (4-8 GHz) for communication. To sample these frequencies accurately, the sampling rate must be at least two times, preferably closer to three times, the carrier frequency being used for communication. These frequencies tend to be beyond most conventional digital converter technology, so analog conversion techniques such as frequency mixing are typically used to convert the received signal to a lower fixed intermediate frequency (IF) to bring the signals within range of standard digital converter technology.

If data conversion technology was fast enough, these signals could be directly sampled by the Analog-to-Digital Converter (ADC), eliminating the need for the front-end mixer. Direct sampling also enables the full bandwidth to be processed using digital signal processing (DSP) techniques.

In order to fully process the generation and reception of SATCOM signals, a large amount of processing is required. Historically this required the development of expensive custom ASICs. As FPGAs have continued to grow in capability, the processing can now be performed by several FPGAs as long as there is sufficient interconnect bandwidth to pass the data between the FPGA processing units. Because FPGAs are reconfigurable, this also enables the design to be upgradeable over time with new algorithms, without changing the hardware.



Example SATCOM system

Recently a major SATCOM provider came to Curtiss-Wright Defense Solutions to see if there was a way to combine the ultra-wideband sampling performance of the multi-gigabit ADCs and DACs with the high-performance FPGA products into a flexible architecture for a SATCOM product. The goal was to create a product that could be used for land-based stations, as well as for simulation of space based stations.

Solution

Curtiss-Wright has worked with Tektronix Component Solutions to develop a set of products that utilize market leading 12 and 25 Gsps ADCs and DACs, enabling direct sampling of both S-band and C-band signals. Curtiss-Wright has taken this technology and brought it into an OpenVPX and high performance embedded computing (HPEC) environment, allowing this technology to be integrated into a system which contains FPGAs, DSP processor modules, GPGPU modules, switches, recorders, and high speed backplanes.

For the S-band system, the CHAMP™-WB-DRFM was chosen as it can support both 12 Gsps ADCs and DACs combined to a single FPGA. Since one FPGA was insufficient to perform the processing required, it required other FPGAs modules and a high bandwidth means to pass data between the modules.

The CHAMP-WB module provides 20 SerDes which are directly connected to the backplane from the FPGA. Since they each can run up to 10.3 Gbps, they provide 200 Gbps of available bandwidth. This module has a single large Virtex-7 FPGA.

The CHAMP-FX4 module provides 40 SerDes which are directly connected to the backplane from three large Virtex-7 FPGAs. These SerDes can also run up to 10.3 Gbps and therefore provide 400 Gbps of available bandwidth.

With so much data passing between cards, even this amount of bandwidth was insufficient. To provide additional support, Curtiss-Wright created a Rear Transition Module (RTM) that split the RX and the TX links into separate connections. This allows the FPGAs to use Xilinx®' simplex Aurora protocol in a unidirectional mode, so that each SerDes TX/RX pair does not have to go to the same module. The RX links can come from one card while the TX links go to a different card, effectively doubling the amount of SerDes bandwidth available when daisy chaining modules together.

A Gen3 Pass-Thru backplanes was used to provide full access to all of the SerDes signals and provide a flexible environment for creating different configurations based on the specific requirements of the application.

Putting all of this together resulted in a system configuration similar to what is shown below. The system contains two CHAMP-FX4s, a CHAMP-WB, and a CHAMP-WB-DRFM, all connected with a set of high speed SerDes between the boards. The dual-ARM® core processor on one of the FX4s controls the CHAMP-WB and CHAMP-WB-DRFM driver.

Results

By combining the industry leading 12 Gsps (and now 25 Gsps) data converter modules with high-performance FPGA products, a SATCOM system can directly sample S-band and C-band signals with a flexible amount of configurable processing sitting behind it. These modules can also be combined with other general purpose processor modules, switch cards, or recorders to provide even more capability.

While this system was specifically created for a SATCOM application, this same concept can be applied to other wideband communication systems that use S-band or C-band frequency signals. This technique can also be applied to higher rate signaling where down conversion may not be able to be eliminated, but it can be simplified.

For signals in the 1-1.5 Gsps range, the VPX3-530 module offers a more compact solution utilizing the 3U VPX form factor. Other rates and resolutions can also be supported by using the full eco-system of available FMC modules directly on the CHAMP-WB or CHAMP-FX4.

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