TECHNICAL NOTE 4019

Factors Affecting System Throughput when Using FibreXtreme SL100/SL240 Cards

Curtiss-Wright Controls Embedded Computing
Data Communication
4126 Linden Avenue
Dayton, Ohio 45432-3068 USA

FAX: 937-258-2729
Phone: 937-252-5601
or 800-252-5601(U.S. only)

Introduction

This Technical Note explains several of the factors that affect system throughput when using FibreXtreme SL100/SL240 cards. The only way to determine actual system throughput is to install FibreXtreme SL100/SL240 cards and measure the throughput. However, consideration of the factors explained in this Technical Note will help to achieve satisfactory system throughput.

Discussion

Many factors affect system throughput when using FibreXtreme SL100/SL240 cards. These factors include, but are not necessarily limited to, the following:

- Link throughput
- FPDP bus throughput
- PCI bus throughput
- System memory bandwidth
- Processing power
- Software driver and application efficiency (e.g., number of threads)
- Operating system
- Computer system. Difference chip sets, etc.

Link Throughput

Link throughput is a function of the link's baud rate and the link's efficiency. FibreXtreme SL100 and SL240 cards have a baud rate of 106.25 MB/s and 250 MB/s, respectively. The link's efficiency is defined as the Data Words in Frame divided by the Total Words in Frame. The total words in frame include both the data words and all overhead words, which are determined by the VITA 17.1 Serial Front Panel Data Port (FPDP) link protocol used by FibreXtreme cards.

The majority of data is transferred in Serial FPDP's Normal Data Fiber Frames, which may contain 0 - 512 32-bit data words. This frame type is least efficient when the optional Cyclical Redundancy Check (CRC) is enabled and the Serial FPDP transmitter is inserting the three extra optional IDLE primitives per frame (i.e. Copy Master Mode is enabled). The three extra IDLE primitives are required when the Serial FPDP transmitter is in a ring topology. Since more overhead words per frame decreases link efficiency, the following calculations assume CRC is enabled and the three extra IDLE primitives are added to each frame. The link is most efficient for full (512 data words) and least efficient for minimal (1 data word) Normal Data Fiber Frames.

Link Efficiency for full (512 data words) data frames
= 512 / 521 = 98.27%

Link Efficiency for minimal (1 data word) data frames
= 1 / 10 = 10.00%

Figure 1 shows the maximum theoretical throughput vs. packet size for SL100 and SL240 links when CRC is enabled and three extra IDLE primitives are added per frame (i.e. Copy Master Mode is enabled). The maximum theoretical throughput is the link's baud rate multiplied by the link's efficiency.

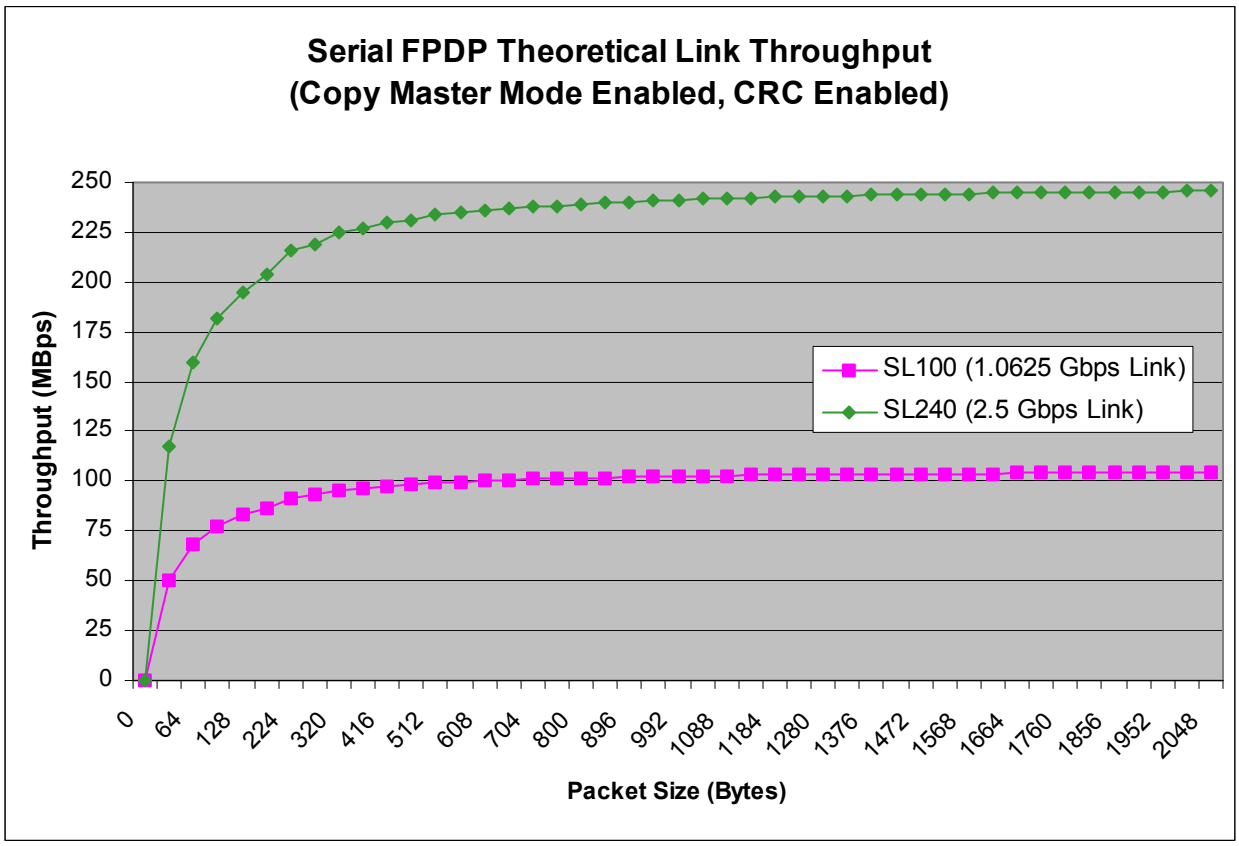

Figure 1 SL100/SL240 Maximum Theoretical Throughput vs. Packet Size

FPDP Bus Throughput

FPDP bus throughput is a function of the FPDP STROBE (or PSTROBE & /PSTROBE) clock. The VITA 17 Front Panel Data Port (FPDP) standard defines two maximum FPDP transmit clock frequencies – 20 MHz (TTL STROBE) and 40 MHz (+/- PECL STROBE). The VITA 17 specification does not define any maximum FPDP receive frequency.

The FPDP bus is a 32-bit (4 bytes) bus. Thus, maximum FPDP-bus transmit throughput, as defined by VITA 17, is

= 20 MHz * 4 bytes = 80 MB/s or
= 40 MHz * 4 bytes = 160 MB/s

Table 1 FPDP Transit Throughput

Card Type	FPDP Transmit Clock Frequency	FPDP Transmit Throughput (Maximum)
SL100 (maximum theoretical link throughput is 105.22 MB/s)	26.5625 MHz	106.25 MB/s
	17.7083 MHz	70.83 MB/s
	13.2813 MHz	53.13 MB/s
	8.8542 MHz	35.42 MB/s

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Card Type	FPDP Transmit Clock Frequency	FPDP Transmit Throughput (Maximum)
SL240 (maximum theoretical link throughput is 247.58 MB/s)	62.5000 MHz	250.00 MB/s
	41.6667 MHz	166.67 MB/s
	31.2500 MHz	125.00 MB/s
	20.8333 MHz	83.33 MB/s
Maximum per VITA 17 specification	40.0000 MHz	160.00 MB/s
	20.0000 MHz	80.00 MB/s

PCI Bus Throughput

The PCI bus can operate in any one of several configurations. Table 2 shows these configurations and the resulting maximum PCI bus throughputs.

Table 2 PCI-Bus Throughput

PCI Bus	PCI-Bus Throughput
32-bit / 33 MHz	132 MB/s
64-bit / 33 MHz	264 MB/s
64-bit / 66 MHz	528 MB/s

However, actual PCI bus throughput is not simply a function of bus width (32 or 64 bits) and bus frequency (33 or 66 MHz). PCI bus throughput is also affected by the following:

- Number of devices on PCI bus. The available PCI bus bandwidth is divided among the devices on the bus.
- The device in control of the PCI bus.
- PCI bus utilization. For example, if the PCI bus is being used for many small transactions, there is more overhead per transaction.
- The slowest device on the bus. A 33 MHz card on a 66 MHz PCI bus will slow all cards on that bus to 33 MHz.
- PCI bus arbitration.
- PCI bridging.

System Memory Bandwidth

Figure 2 shows an example sensor-to-storage (STS) system. STS applications import data from a sensor across a Serial FPDP link via a special Host Bus Adapter (HBA), and then export the data to a storage device. The CPU is connected to system memory (RAM) via the system bus. All data normally must pass through RAM. Data is acquired from the link is Direct Memory Accessed (DMA'ed) across the PCI bus to the RAM on the system bus (Figure 2, item ①). The Fibre Channel (FC) HBA storage device then DMA's the data out of RAM through the system bus and the PCI bus (Figure 2, item ②). The bottleneck is the extra copy of the data across the busses.

The system memory type (e.g., SDRAM, DDR SDRAM, RAMBUS, etc.) and the system bus frequency and data width also affect the data throughput between the CPU and system memory.

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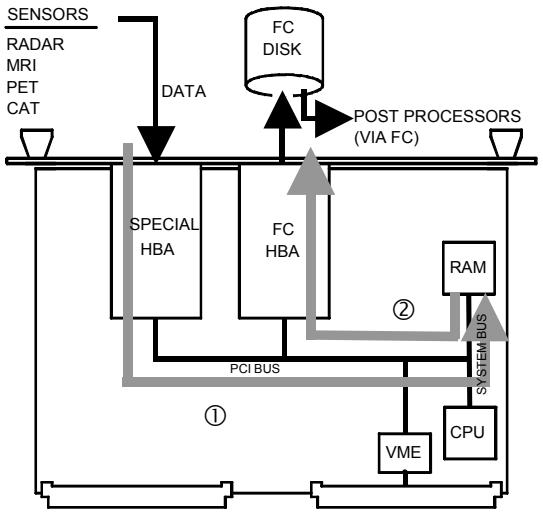

Figure 2 Normal Data Flow in a Sensor-to-Storage (STS) System

Processing Power

CPU speed is well recognized as an important benchmark of a computer system. Usually faster is better, but that is not the whole story. Whether the CPU is performing calculations or data reduction or simply moving the data to a storage device determines how critical CPU speed is to system throughput. Also, CPU read time and write time are not necessarily identical. This could result in faster receive throughput than transmit throughput or vice versa.

Software Driver and Application Efficiency (e.g., Number of Threads)

Software drivers and applications also affect system throughput. Well-written drivers and applications using multiple threads may be more efficient and allow higher system throughput as the multi-threading allows a greater degree of concurrency within the system. This results in potential advantages in resource utilization. The method of using SL100/SL240 data buffers also has an impact on system throughput. The process is tied up during data movement (blocking driver).

Operating System

All operating systems are not created equal. Operating systems differ in their interrupt latency, virtual to physical address translation, memory locking, semaphores, maintenance of cache coherency, context switching between processes and process priority, and amount of overhead.

Computer System (e.g., Different Chip Sets, etc.)

All computer systems are not created equal. Some of the differences in computer systems were explained above (e.g., PCI bus throughput, system memory bandwidth, and processing power). The agent maintaining cache coherency also affects system throughput; i.e., the hardware or the operating system.

Conclusion

This Technical Note explained several of the factors that affect system throughput when using FibreXtreme SL100/SL240 cards. The system designer has some control over several of these factors (e.g., link throughput, FPDP bus throughput, and PCI bus throughput). However, the system designer has less control over various other factors (e.g., operating system, different chip sets in the computer system). The only way to determine actual system throughput is to install FibreXtreme SL100/SL240 cards and measure the throughput. However, consideration of the factors explained in this Technical Note will help to achieve satisfactory system throughput.

Related Information

- *FibreXtreme SL100/SL240 Hardware Reference Manual for PCI, PMC, and CPCI Cards,* (Doc. No. F-T-MR-S2PCIPMC), Systran Corporation.

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- *FibreXtreme SL100/SL240 Hardware Reference for VME and Rehostable CMC FPDP Cards*, (Doc. No. F-T-MR-S2fpdp##), Systran Corporation.
- *Serial Front Panel Data Port (FPDP) Standard, VITA 17.1*, Revision 0.8a; October 16, 2002. Produced by the VITA Standards Organization.
- *Front Panel Data Port (FPDP) Specifications, ANSI/VITA 17-1998, Revision 1.0*; February 11, 1999. Produced by the VITA Standards Organization.
- *PCI Local Bus Specification,* Revision 2.2, December 18, 1998; PCI Special Interest Group.

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