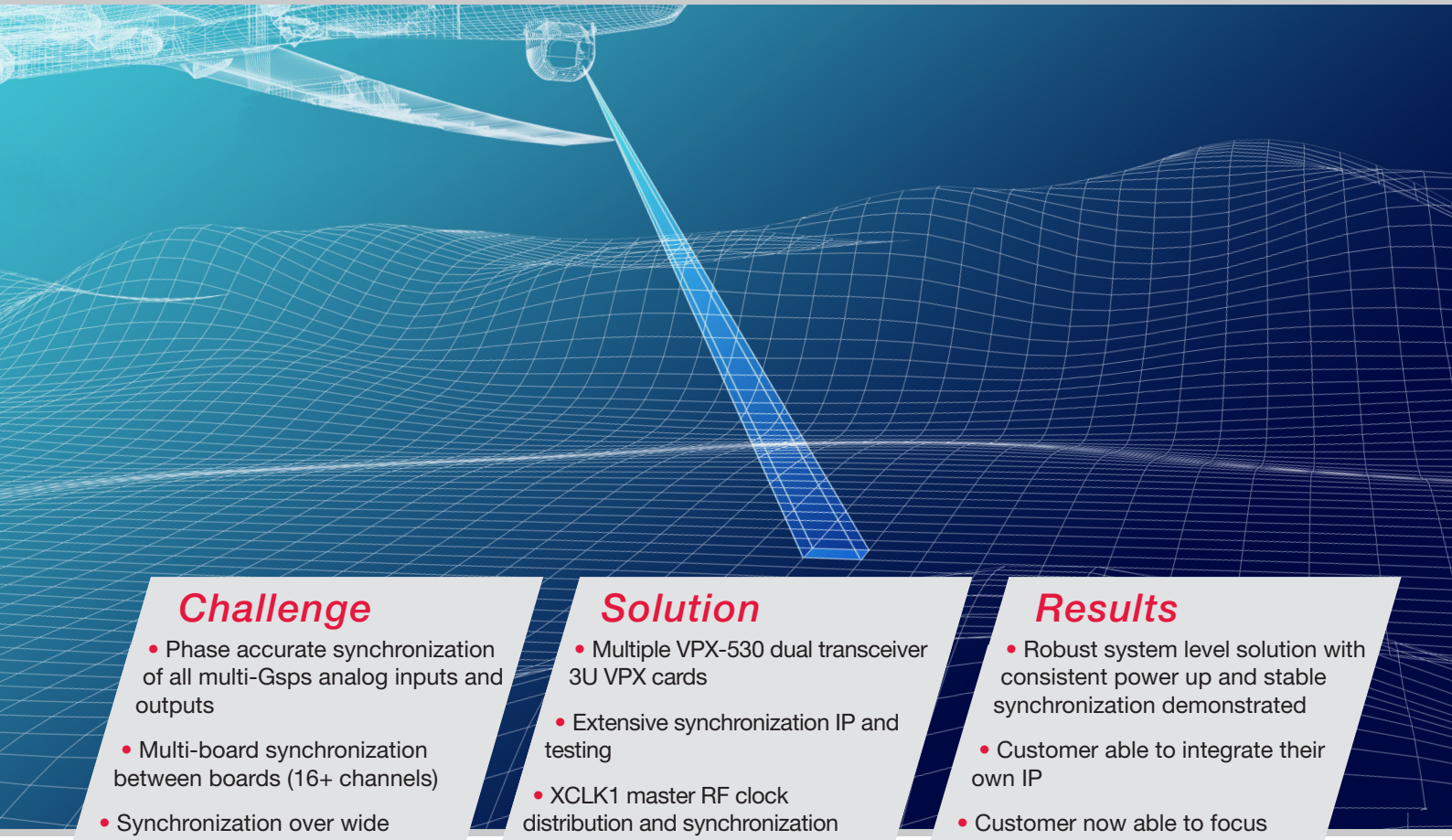
CASE STUDY

# Multi-Gsps, Multi-board Analog IO Synchronization

CURTISS-WRIGHT

DEFENSE SOLUTIONS



## Challenge

- Phase accurate synchronization of all multi-Gsps analog inputs and outputs
- Multi-board synchronization between boards (16+ channels)
- Synchronization over wide temperature ranges

## Solution

- Multiple VPX-530 dual transceiver 3U VPX cards
- Extensive synchronization IP and testing
- XCLK1 master RF clock distribution and synchronization control

## Results

- Robust system level solution with consistent power up and stable synchronization demonstrated
- Customer able to integrate their own IP
- Customer now able to focus their efforts on their application itself

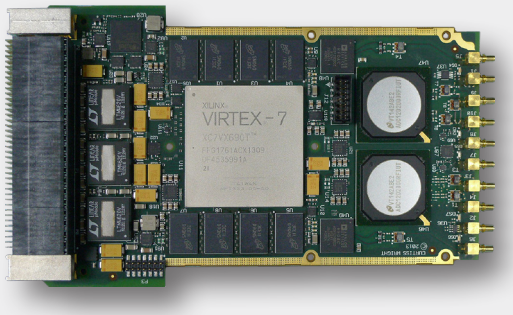
## Challenge

Some problems can be difficult to solve. Phase accurate synchronization of analog signals through multiple analog to digital converters at multi-GHz rates on a single card is one such problem. Synchronization between multi-boards or systems raises the bar even further. To do this over wide temperature ranges reliably takes the problem up yet another notch.

The challenge was to achieve all of these with eight Curtiss-Wright's VPX3-530 transceivers; each with four 2 Gsps data converters, a total of 32 analog input channels requiring cycle accurate synchronization. The VPX3-530 has also dual analog outputs for a total of 16 analog output, all demanding synchronization.

## Solution

The VPX3-530 was designed for synchronization; to do this with eight cards is unusual, but powerful and therefore likely to become more common. Each VPX3-530 requires an external master reference clock. This system uses a Curtiss-Wright XCLK1. The XCLK1 provides two key advantages. The first distributes a high quality phase aligned clock at the RF sample frequency. Not having to rely on PLL frequency multiplication at the RF clock distribution stage means that the sample clock is common based and locked to every other clock with no chance of extra clock cycles being added. This ensures the clock stage remains in sync. The second advantage of the XCLK1 is that it can be momentarily stopped.




VPX3-530 Dual Transceiver

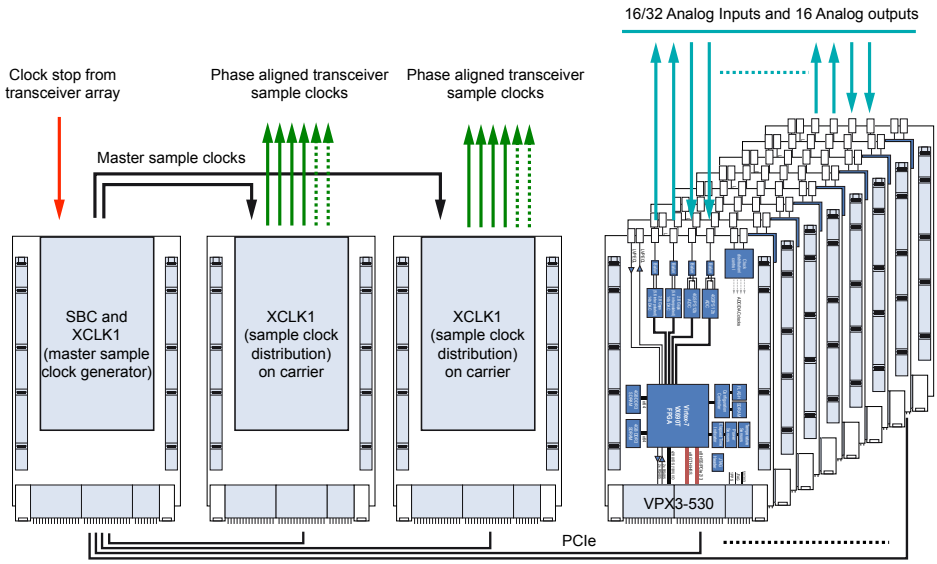
The VPX3-530 exploits the clock stopping mechanism to stop the sample clocks to the RF ADCs thereby halting the data conversions under the control of the card's FPGA. A typical synchronization sequence starts with a user command, usually during power up, to all FPGAs (all VPX3-530 cards). One of these cards is designated to be the sync master. The sync master stops the RF sample clock (XCLK1). After this the VPX3-530's FPGA flushes the data pipes/FIFO/buffers, including both ADC and FPGA devices, thereby providing onboard synchronized data from analog input to DMA data output. When the final slave VPX3-530 has completed this cycle, the XCLK1 is released and the ADCs start to convert again. Since the ADCs continually convert, this means all boards are now in sync and will continue to be in sync. This technique is used with other Curtiss-Wright data converter products. In the case of the VPX3-530, however, the LSB of the data converter is also used, via the sync input signal. The backend digital interface on the VPX3-530 recognizes this bit being changed the instant the external sync signal is asserted, ensuring the data flow is coherent.

One minor issue with the current generation of XCLK1 is that the number of outputs is limited to six RF clock outputs, but eight are required. Usefully, the XCLK1 can be clocked in a number of modes; two being master RF clock generation, using either an onboard TXCO or external reference, or a simple RF clock distribution mode. For eight outputs, three XCLK1s are used. One XCLK1 is the master RF clock generator and two others are used to provide RF clock distribution for up to 12 outputs. Though only a second XCLK1 is needed to provide the necessary number of outputs, two additional XCLKs help to equalize the RF clock signal chain lengths. The XCLK1 was designed to be able to be scaled in this manner.

## Results

Although the solution outlined looks simple, timing challenges are very tight from ADCs, which can be stopped for a very short time, to fast pipeline flushing and fast coordination between FPGAs.

After a lot of engineering design, a robust system level solution was delivered with consistent power up and stable synchronization demonstrated. This allowed the customer to develop their own software using an external SBC and HDL in an FPGA shared with the synchronization IP. Though a critical concern for the customer, they did not have to develop their own specific code and verify the design to achieve multi-channel, multi-card synchronization nor worry about card level interoperability, but instead focus their efforts on their application itself. A big problem solved.




System Outline Block Diagram
(inter VPX3-530 trig in/out daisy chain not shown)

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