Panavia

This paper introduces the Panavia bus, focusing on its physical layer as well as word definition and tag sequence.

The following topics are discussed:

5.1 Overview

Mainly used on the Tornado, Panavia is a single-source (Tx) single-sink (Rx) architecture (see the following figure). All data is transmitted over two twisted pairs in one direction only. One twisted pair is for data (NRZ-L) and the other is for a (64 kHz) data clock.

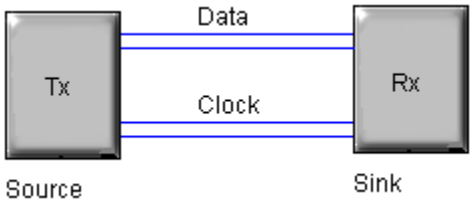

Figure 5-1: The Panavia bus transmits point-to-point in one direction

Data is sent in 32-bit words, each identified by one of 32 5-bit tags.

5.2 The physical layer

Data is transmitted in a Non Return to Zero-Level (NRZ-L) format with a data clock. The last 6 transmitted bit periods on the data line are *clocks* (illegal NRZ-L bits). The three types of bit are illustrated in the following figure.

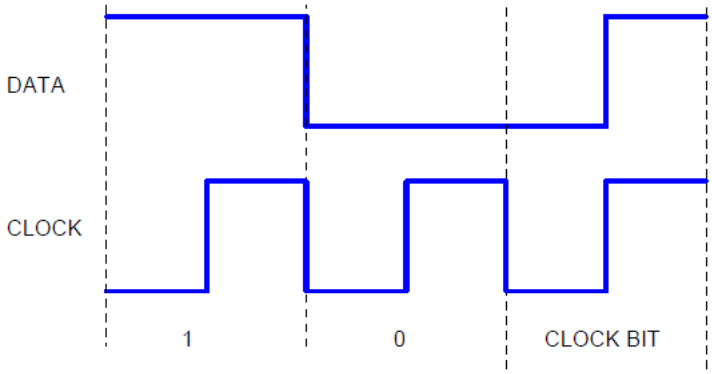

Figure 5-2: The Panavia code for 1, 0 and clock

Data transfer is at 64 kHz, and for a transmitter the high voltage must be between +3.5 and 5.5V.

5.3 Word definition

The following figure illustrates the bit definition of a Panavia word.

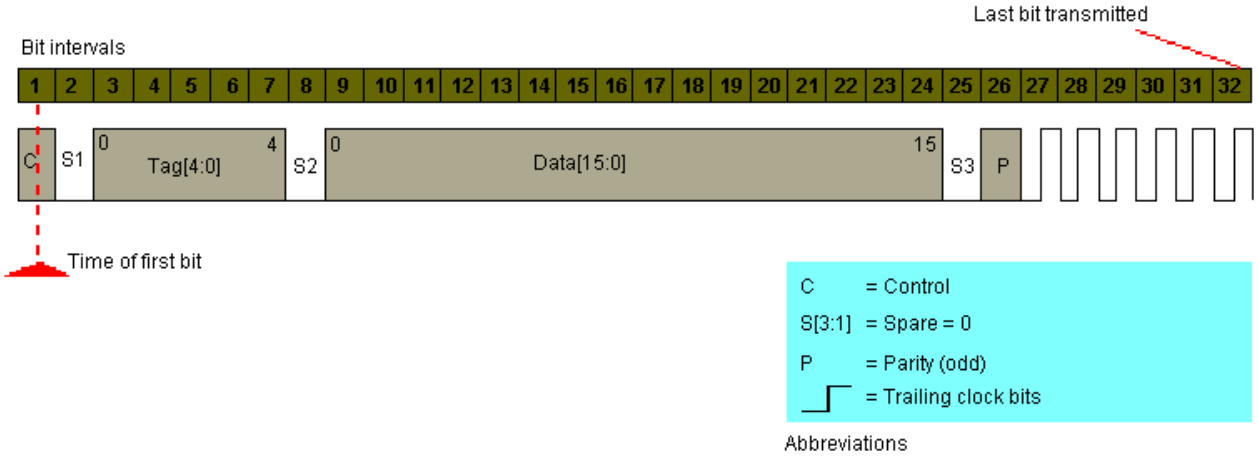

Figure 5-3: Word definition for Panavia

The 5-bit tag identifies the parameter being transmitted. Tags can start at 0 decimal and end with 31 decimal. Tags are transmitted in a sequence and must increase then wrap around.

5.4 Conclusion

In this paper, some of the nomenclature associated with Panavia was introduced. The generic word definition was also discussed.